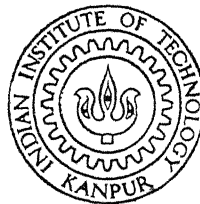


DEVELOPMENT OF A SOFTWARE PACKAGE FOR SWITCHED CAPACITOR FILTER DESIGN

by

SUBHASHISH MUKHERJEE



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY KANPUR
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FOR
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in Partial Fulfilment of the Requirements
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by
SUBHASHISH MUKHERJEE

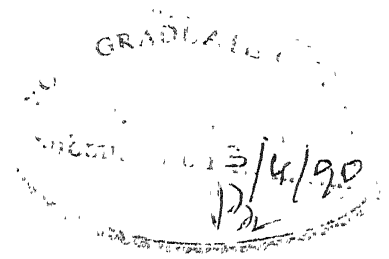
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CERTIFICATE

This is to certify that this thesis titled "DEVELOPMENT OF A SOFTWARE PACKAGE FOR SWITCHED CAPACITOR FILTER DESIGN" is a report of work carried out under my supervision by Mr. Subhashish Mukherjee and that it has not been submitted elsewhere for a degree.

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ABSTRACT

In this work, **SFDP**, a software package for the design of *switched capacitor filters*, has been developed. **SFDP** can generate circuit schematics from frequency domain specifications. The design approach has been to first derive an s-domain *elliptic filter transfer function* from specifications. This is then transformed to the z-domain using the *bilinear s-to-z transformation*. The z-domain transfer function is then matched with the transfer functions of standard switched capacitor *biquad building blocks* to obtain the circuit component values. A sub-module to design the *operational amplifiers*, used in the filter circuits, has also been included in the package. Several designs have been performed using **SFDP** and some of the designed circuits have been simulated using **SPICE**.

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CHAPTER 1

INTRODUCTION

In this chapter, the basic concept of a *switched capacitor* (SC) performing as a simulated resistor is introduced. The advantages, disadvantages and area of application of such circuits are briefly discussed. An outline of the present work, a software package developed for the design of switched capacitor filters, is given. Finally, the organization of this thesis is outlined.

1.1 SWITCHED CAPACITOR CIRCUITS

Advancements of MOS technology in digital circuits has led to the development of LSI and VLSI systems. MOS analog circuits are also finding their use in the VLSI systems. Systems are being developed which use both digital and analog circuits on the same chip. Following these developments, design of subsystem modules using analog MOS VLSI has become an active area of research. Among the various modules, automated design of switched capacitor filters has been condensed in this thesis.

The use of MOS technology in switched capacitor circuits was first proposed by Fried [1] and has been improved by many other researchers [2],[3],[4]. Switched capacitor circuits are a special class of *sampled data analog systems* where a signal is represented by the uncoded amplitude of an electrical quantity (normally, a voltage) as in an analog system. However, the system contains a clock, and the signal amplitude is sensed only at discrete time instances, as in a digital system. The clock is used mainly to simulate a resistor by periodically charging and discharging a capacitor. MOSFETs are used as switches for this purpose.

The following figure shows how resistors can be simulated using capacitors and switches.

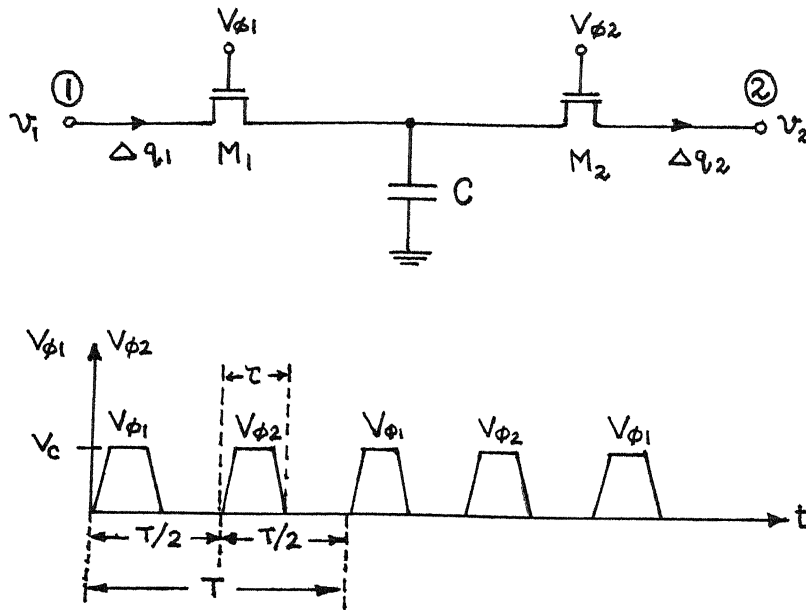


Figure 1.1. Simulated Resistor: (a) Circuit Diagram (b) Clock Waveforms.

The figure shows a circuit with two MOS switches M_1 and M_2 and a capacitor C . Figure (1.1b) shows the clock pulses $V_{\phi 1}$ and $V_{\phi 2}$ activating the MOSFETs. Whenever $V_{\phi 1}$ equals V_c , M_1 is in full conduction providing a low resistance between source and drain. When $V_{\phi 1}$ is zero, M_1 acts as open circuit. M_2 is similarly driven by $V_{\phi 2}$. Assume that v_1 and v_2 are slowly varying during a clock interval T (fig. 1.1b), i.e., they do not change appreciably. This will be the case if the highest frequency components of v_1 and v_2 are much smaller than the clock frequency $1/T$.

Next, consider in fig. 1.1a the charge Δq_1 entering C from the input terminal as $V_{\phi 1}$ rises to V_c . Since C was previously charged to v_2 , $\Delta q_1 = C(v_1 - v_2)$. Next $V_{\phi 1} \rightarrow 0$, M_1 cuts off and C holds its voltage at v_1 . When now $V_{\phi 2} \rightarrow V_c$, C is recharged to v_2 again through M_2 . Then $\Delta q_2 = C(v_1 - v_2) = \Delta q_1$. Since at each clock interval T a charge $C(v_1 - v_2)$ enters at node (1) and leaves at node (2), we can define the average current i flowing from (1) to (2) as

$$i = \frac{\Delta q_1}{T} = \frac{\Delta q_2}{T} = \frac{C}{T} (v_1 - v_2) \quad (1.1)$$

or equivalently $i = (v_1 - v_2)/R$ where $R = T/C$. Thus the average current i and the voltage difference $(v_1 - v_2)$ satisfies Ohm's Law and the circuit of figure (1.1a) behaves as a resistor of value $R = T/C$ ohms.

For integration, SC circuits are superior to other analog circuit

implementations, e.g., an active RC circuit. SC circuits need much less chip area because of the following reasons. To achieve an RC time constant in the audio frequency range (say, 10 K rads/s) using an active RC circuit, even with a large (10 pF) capacitor, a resistance of 10 M Ω is required. Such a resistor will occupy an area of about $10^6 \mu\text{m}^2$, which is prohibitively large. By contrast, for a typical clock period of $T = 10 \mu\text{s}$, the capacitance for realizing a 10 M Ω resistor is about $C = T/R = 1\text{pF}$. The area required to realize this capacitance is about $2500 \mu\text{m}^2$, only about 0.25% of that needed by the resistor that which it replaces.

Another major advantage over fully analog implementation is that in an SC circuit all time constants will be given by expressions of the form $(T/C_1)C_2 = T(C_2/C_1)$. Here, the clock period T is usually determined by a quartz crystal controlled clock circuit, and is hence very accurate and stable. The other factor (C_2/C_1) is the ratio of two on chip MOS capacitances. It is possible to obtain an accuracy and stability of the order of 0.1% for this ratio (*tracking error*). Since capacitors are made in different fabrication steps than resistors, their errors do not track with those of the resistors on the same chip. The errors of capacitors and resistors are of the same order, that is, about 10% individual error. Hence for an expression of time constant of the form RC as in an analog circuit, the error in RC can be as large as 20%. Thus the overall accuracy of an SC circuit is at least a hundred times better than what can be achieved with an on chip resistor and capacitor for the RC time constant.

In SC circuits, since only periodic samples of the signals are of interest, it is possible to time share (multiplex) the whole circuit, or parts such as the op-amps of the circuit, among several signal channels resulting in highly efficient multichannel systems. Also all time constants of an SC circuit are proportional to the clock period T . As a result, the overall gain versus frequency response $H(f)$ can readily be scaled by changing the clock frequency $f_c = 1/T$. This gives a valuable tool for fine tuning of the response for applications such as voltage controlled oscillators, adaptive filters, tracking filters, and so on. Another major advantage of SC circuit is that it is fabricated using standard MOS technology and can share the area on the same chip with digital circuitry.

As SC circuits handle signals in analog forms, the basic operations (multiplication, addition, delay) needed in signal processing are much simpler to perform than in digital circuits. Hence, the density of operation on the chip can be much higher than for digital signal processors. Also due to the basic simplicity

of the circuits, the speed with which signal processing tasks can be accomplished is much higher than for digital systems. Due to much simpler structure, the chip area needed and the dc power required for a given signal processing task is also considerably less for an SC implementation than for a digital one.

One major disadvantage of SC circuits as compared to digital signal processors is their limited accuracy. As mentioned earlier, the capacitance ratios (which determine the coefficients and thus poles and zeros of the transfer functions) can be made accurate and stable to about 0.1% accuracy of their nominal values. This only corresponds to about 10-bit floating point accuracy in digital terms. For some applications, this precision is not sufficient, and (say) a 16-bit accuracy is mandatory, precluding the use of SC circuits. Due to relatively large level of noise originating from the op-amps and switches, and also coupled from the clock and the supply lines, and so on, the dynamic range of SC circuits seldom exceeds 100 dB; values of 70 - 90 dB are common. The corresponding range for a digital filter is much larger.

The above mentioned advantages has led to wide applications of SC circuits in telecommunication systems. Main applications of these circuits are in frequency selective filtering. Other applications are in analog to digital and digital to analog data conversion, Programmable gain amplification for AGC and other applications, nonlinear applications as multiplication, modulation, detection, rectification etc. They have also been used extensively in large mixed analog digital systems such as codecs, modems and speech processors [5],[6].

1.2 AUTOMATED DESIGN OF SC FILTERS

As mentioned above, frequency selective filtering is the major application of SC circuits. Design of such a filter is a complex procedure consisting of several steps. Thus use of computer becomes necessary for fast and error free design. In the present work a software package, called SFDP → *Switched capacitor filter design package*, has been developed which designs SC filters from given user specifications using *coupled biquad structures*. There are many possible ways of designing an SCF [15] which meets the user specifications, as shown in table (1.1). The steps that have been followed are highlighted. The software has been developed using well established theories and standard approaches. This ensures

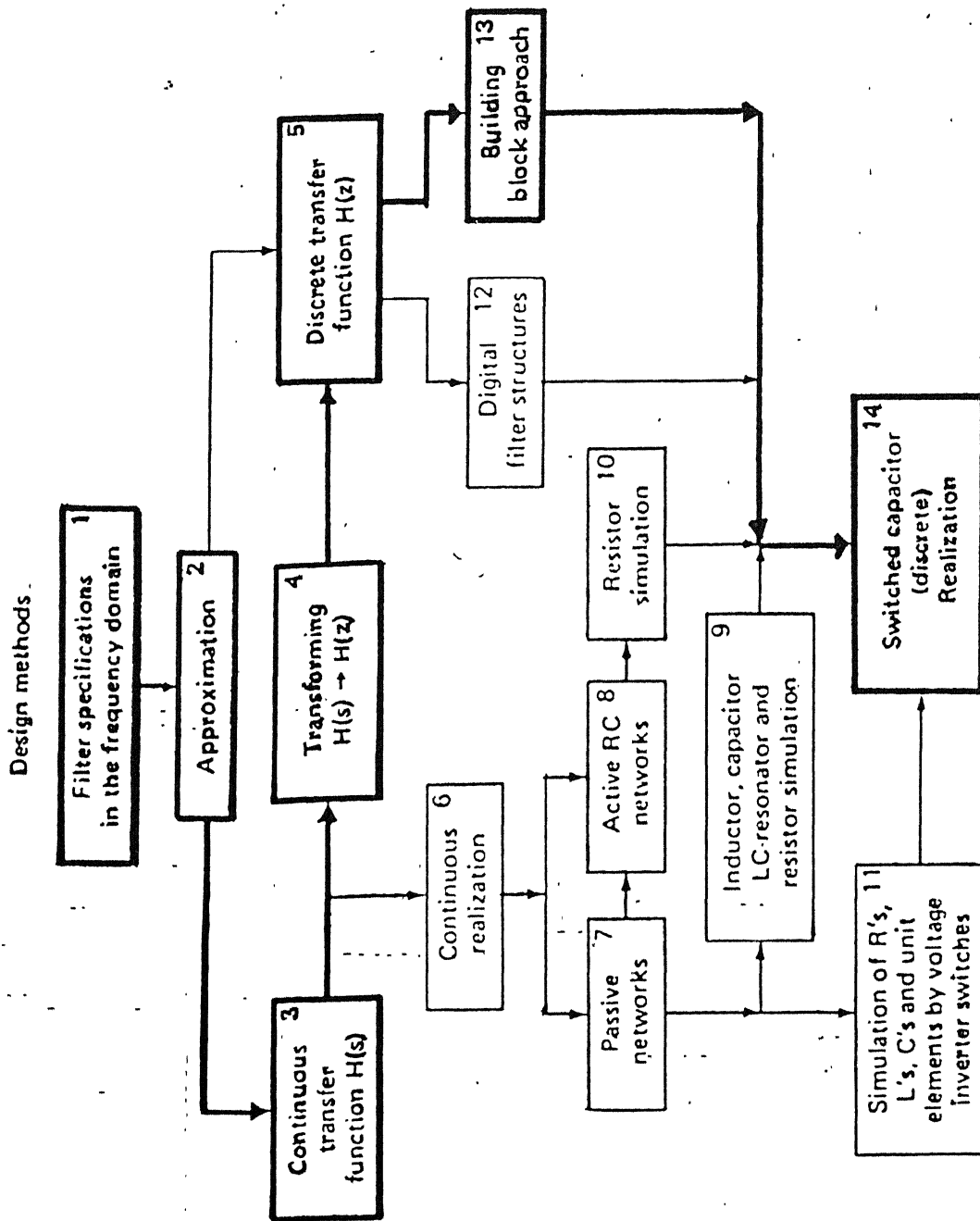


Table 1.1. Design methods for SC filters. The steps followed are highlighted.

error free design and trouble free implementation.

The user specifications are given as an input file to SFDP. The designed filter circuit along with various other informations are given as an output file. The input specifications consist of required frequency domain characteristics of the filter. Also specifications for the operational amplifiers to be used in the circuit may be given. SFDP then designs the op-amp from these specifications which is then used in the filter design.

Using the input specifications, first an *s domain elliptic filter transfer function* is synthesized. This *s domain* transfer function is then split into biquadratic blocks. To optimize filter performance, *pole-zero pairing* is performed so as to satisfy certain optimization criteria. After forming the biquads they are *reordered* to maximize filter performance. This transfer function is then transformed into the *z transform* domain using the *bilinear s-to-z transformation*. The *z domain* biquad blocks are then matched with the transfer functions of standard SC biquad blocks. The choice of a biquad structure depends on the nature of the *z domain* transfer functions. Thus from matching the coefficients of the two transfer functions initial values of all the circuit components are found. Then *scaling* and fine tuning of these values are performed, which helps in improving filter performance and reduces the area requirement for implementing the filter. Finally, the designed circuit, along with all other required informations, is printed out as an output file in tabular form.

1.3 ORGANIZATION OF THE THESIS

In **chapter 2**, the theory to synthesize an elliptic filter transfer function from given specifications is discussed. The issues related to pole-zero pairing, required to split a transfer function into biquadratic blocks, and ordering of these biquads are also considered.

In **chapter 3**, the necessary theory to design SC filter circuits from given *s domain* transfer functions is presented. The bilinear *s-to-z* transformation is discussed followed by a discussion on switched capacitor circuits. Then standard SC biquad building blocks are described. The important issue of the scaling of SC circuits is considered next. The chapter is concluded with a brief discussion on

different nonlinear effects that affect filter performance.

In chapter 4, MOS operational amplifier circuits are discussed. The chapter starts with the description of analog circuit building blocks that are used to design an op-amp. This is followed by the description of different op-amp circuits that can be designed using SFDP. Finally, a step by step description of the procedure to design an op-amp from given user specifications is given.

In chapter 5, the organization of SFDP is described. This is followed by some design examples that has been done using SFDP. SPICE simulation results of some of the designed circuits are provided.

In chapter 6, we present conclusions.

A user manual for SFDP has been included in the appendix.

CHAPTER - 2

ANALOG FILTERS

In this chapter we will be considering the approximation problem for filter design. We will try to derive transfer functions of filters from given input specifications and will discuss about subsequent modifications of these transfer functions needed to realize physical filters.

2.1. BASIC CONCEPTS [7],[8]

The figure below shows a filter as a black box. It is characterized in the time domain by its impulse response $h(t)$, which is the output signal $y(t)$, produced in response to a unit impulse $\delta(t)$, applied at the input.

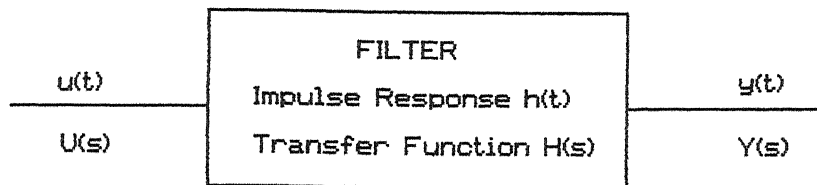


Fig. 2.1. Black Box Representation of a Filter.

For an arbitrary input signal $u(t)$, the output signal $y(t)$ is given by the convolution integral

$$y(t) = \int_{-\infty}^{+\infty} h(t - \tau) u(\tau) d\tau \quad (2.1)$$

The transfer function of the filter $H(s)$ is given by the unilateral Laplace Transform of $h(t)$, defined as

$$H(s) = \int_0^{\infty} h(t) e^{-st} dt \quad (2.2)$$

By Laplace transform of (2.1) we get $Y(s) = H(s)U(s)$. Thus the system transfer function $H(s)$ is given by,

$$H(s) = \frac{Y(s)}{U(s)} = \frac{\text{output variable}}{\text{input variable}} \quad (2.3)$$

From the theory of linear systems we get that $H(s)$ in the most general case will be a real rational polynomial function of the complex variable s . Thus in general

$$H(s) = P(s)/Q(s) = \frac{p_0 + p_1 s + \dots + p_{m-1} s^{m-1} + p_m s^m}{q_0 + q_1 s + \dots + q_{n-1} s^{n-1} + q_n s^n} = \frac{\sum_{i=0}^m p_i s^i}{\sum_{i=0}^n q_i s^i} \quad (2.4)$$

where p_i and q_i are real numbers.

$H(s)$ is real for real s and the roots of the polynomials $P(s)$ and $Q(s)$ must either be real or occur in conjugate pairs. In general, for the types of transfer functions we shall consider, the degree of numerator is equal to or less than the degree of denominator ($m \leq n$) and $Q(s)$ is a strictly Hurwitz Polynomial. $Q(s)$ is called the characteristic polynomial or natural mode polynomial of the linear system and the degree of $Q(s)$, i.e. n , is the order or degree of the system.

One may obtain the frequency behavior of $H(s)$ by letting $s=j\omega$ and evaluating $H(s)$ along the imaginary axis,

$$(H(s))_{s=j\omega} = H(j\omega) = P(j\omega) / Q(j\omega) \quad (2.5)$$

Thus,

$$H(j\omega) = \text{Re}\{H(j\omega)\} + j \text{Im}\{H(j\omega)\} \quad (2.6)$$

$$= |H(j\omega)| e^{-j\phi(\omega)} \quad (2.7)$$

where $|H(j\omega)|$ is the magnitude and $\phi(\omega)$ is the phase of $H(j\omega)$. $\phi(\omega)$ is obtained as

$$\phi(\omega) = \tan^{-1} [\text{Im}\{h(j\omega)\} / \text{Re}\{H(j\omega)\}] \quad (2.8)$$

In the following sections we will more frequently use the transfer function $G(s)$, which is the inverse of $H(s)$, the system transfer function. Thus

$$G(s) = \frac{1}{H(s)} = \frac{E(s)}{P(s)} = \frac{\text{input variable}}{\text{output variable}} \quad (2.9)$$

In $G(s)$ the roles of poles and zeros are reversed to that of $H(s)$. Note that while $H(s)$ is a measure of the transmission through the system, $G(s)$ is a measure of the loss through the system.

It is usual practice to obtain a transfer function $G(s)$ whose magnitude approximates unity over the passband. But it is usually a simpler task to obtain rational functions which approximates zero rather than unity. Towards this end, we use the function $K(s)$, called the characteristic function, defined by,

$$|G(j\omega)|^2 = 1 + |K(j\omega)|^2 \quad (2.10)$$

Thus $|K(j\omega)|$ approximates zero when $|G(j\omega)|$ approaches unity. Using analytic continuation we obtain

$$G(s)G(-s) = 1 + K(s)K(-s) \quad (2.11)$$

This equation is central to the design of filters and is known as Feldtkeller's equation. As can be seen, $K(s)$ is also a rational polynomial function and thus can be represented as,

$$K(s)K(-s) = \epsilon^2 \frac{F(s)F(-s)}{P(s)P(-s)} \quad (2.12)$$

$F(s)$ is called the reflection zero or attenuation zero polynomial and $\epsilon = |K(j\omega)|_{\max}$ gives the maximum deviation over the passband of the filter. Thus using (2.10) and (2.11) Feldtkeller's equation can also be written as

$$Q(s)Q(-s) = P(s)P(-s) + \epsilon^2 F(s)F(-s) \quad (2.13)$$

The transfer functions for filters in the s domain suffer from their numerical ill-conditioning. This is because of the clustering of the roots of the polynomial near the band edges. To circumvent this problem a transform which we will call the \hat{z} transform [10] is used. It is defined by,

$$\hat{z}^2 = \frac{s^2 + 1}{s^2 + a^2} \quad (2.14)$$

which is the bilinear mapping between the squared variables. This transform maps the passband edges of a filter $a \leq |\omega| \leq 1$ onto the entire imaginary axis of the

new plane, as shown in figure (2.2).

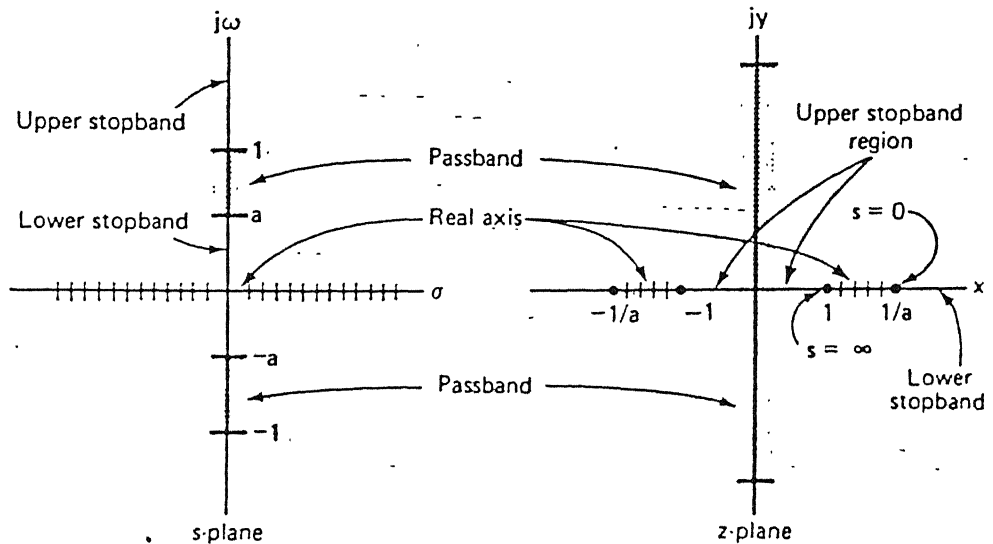


Figure 2.2. Mapping between the s-plane and the \hat{z} -plane

Thus this transform separates the poles alleviating the difficult numerical situation which arise due to the clustering. In the \hat{z} domain one can write the characteristic function as

$$\hat{K}(\hat{z}) \hat{K}(-\hat{z}) = \epsilon^2 \frac{\hat{F}(\hat{z}) \hat{F}(-\hat{z})}{\hat{P}(\hat{z}) \hat{P}(-\hat{z})} \quad (2.15)$$

2.2. THE APPROXIMATION PROBLEM [10]

The filter design problem can be stated as follows: given an input signal $u(t)$ and a desired output signal $y(t)$, first find the impulse response $h(t)$ which satisfies (2.1) and then realize a physical system with an impulse response $h(t)$. Or equivalently, from given input specifications in the frequency domain, one has to derive a transfer function $H(s)$ which satisfies the input specifications. But there may not be a physical system having such an impulse response $h(t)$ and a corresponding transfer function and thus one has to find a function $h^*(t)$ or a

corresponding $H^*(s)$, which is realizable and approximates $h(t)$ or $H(s)$ in certain way. Thus the filter design process can be split into two parts : (1) Approximation phase, consists of finding a realizable transfer function which approximates the given specifications and (2) Realization phase, deals with the synthesis of a physical network. In this chapter we will consider only step (1).

2.2.1 FILTER CLASSIFICATION AND SPECIFICATIONS

Filter transfer functions can be classified in terms of their attenuation characteristics over the frequency axis. The four most common types of filter functions are

- (1) Low Pass (LP) (2) High Pass (HP)
- (3) Band Pass (BP) and (4) Band Reject (BR).

Ideal sketches of attenuation versus frequency for these four types of filters are shown in figure (2.3). As shown, each filter has a well defined passband over which the attenuation is ideally zero db and a well defined stopband in which the attenuation is ideally infinite. But as stated earlier this is not physically realizable. Also the attenuations are not constant over the bands and suffer from variations called ripples. This distortion is not allowable in the sense that frequencies which we wish to pass through the filter will suffer different amount of attenuations. To circumvent this problem, the maximum allowed variation in attenuation over the passband A_p db and the minimum attenuation required over the stopband A_s db are specified. Thus, typically, input specifications consist of

(a) For LOW PASS and HIGH PASS filters :

- (1) Stopband edge f_s in hertz,
- (2) Passband edge f_p in hertz,
- (3) Minimum stopband attenuation A_s ,
- and (4) Maximum passband attenuation A_p .

(b) For BAND PASS and BAND REJECT filters :

- (1) Stopband edges f_{s1} and f_{s2} in hertz,
- (2) Passband edges f_{p1} and f_{p2} in hertz,
- (3) Minimum stopband attenuation A_s ,
- and (4) Maximum passband attenuation A_p .

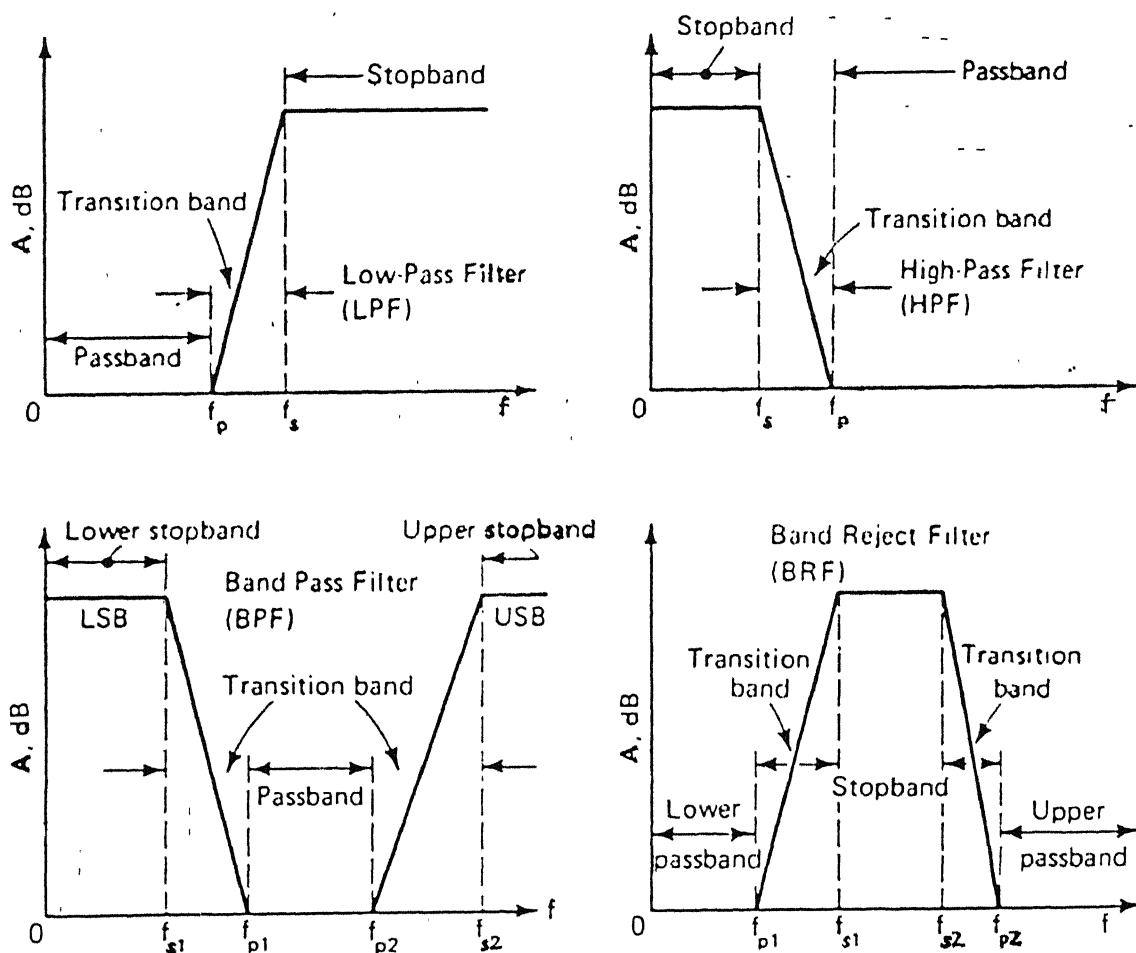


Figure 2.3. Attenuation characteristics of the four types of filters.

One can obtain relation between A_p and ϵ defined in equation (2.12) as follows:

$$\text{Attenuation} \quad A(\omega) = 10 \log_{10} (1 + \epsilon^2)$$

$$\text{giving} \quad \epsilon = [10^{A_p/10} - 1]^{\frac{1}{2}} \quad (2.16)$$

The frequency band(s) separating stopband(s) and passband(s) is called the transition band and should ideally be zero. But for physically realizable filters it is of nonzero value and the narrower the required transition band width is, the higher will be the order of the designed filter leading to a complex and costly realization.

In the actual design procedure, filters are not designed from the specifications directly. First a Low Pass Prototype (LPP) is formed from the given specifications. The LPP is found by normalizing the frequency scale with respect to some suitable frequency making the passband edge of the LPP to be unity. How this is done we will discuss in the next section. Using this new set of normalized specifications a low pass prototype filter (LPP) is found. Then using frequency transformations, also to be discussed in the next section, actual filter transfer functions are obtained. Now we will consider the methods to obtain such LPPs.

2.2.2. ELLIPTIC FILTER APPROXIMATION

There are many approximations possible which can be used to get transfer functions from given LPP specifications. Some of them are

- (1) Butterworth approximation (2) Chebyshev approximation
- (3) Inverse Chebyshev approximation and (4) Elliptic approximation.

Typical attenuation characteristics obtained from these approximations are shown in figure (2.4). Of these the elliptic filter approximation is the most efficient, that is, given A_p , A_s and ϵ , the elliptic filter approximation will give the lowest order n . We will now develop an algorithm to derive filter transfer functions using the elliptic filter approximation.

For elliptic filter approximation, passband attenuation is equiripple. It can be shown that for equiripple passband,

$$\hat{K}(\hat{z}) \hat{K}(z) = \epsilon^2 \frac{[\hat{P}_{ev}(\hat{z})]^2}{\hat{P}(\hat{z}) \hat{P}(-\hat{z})} \quad (2.18)$$

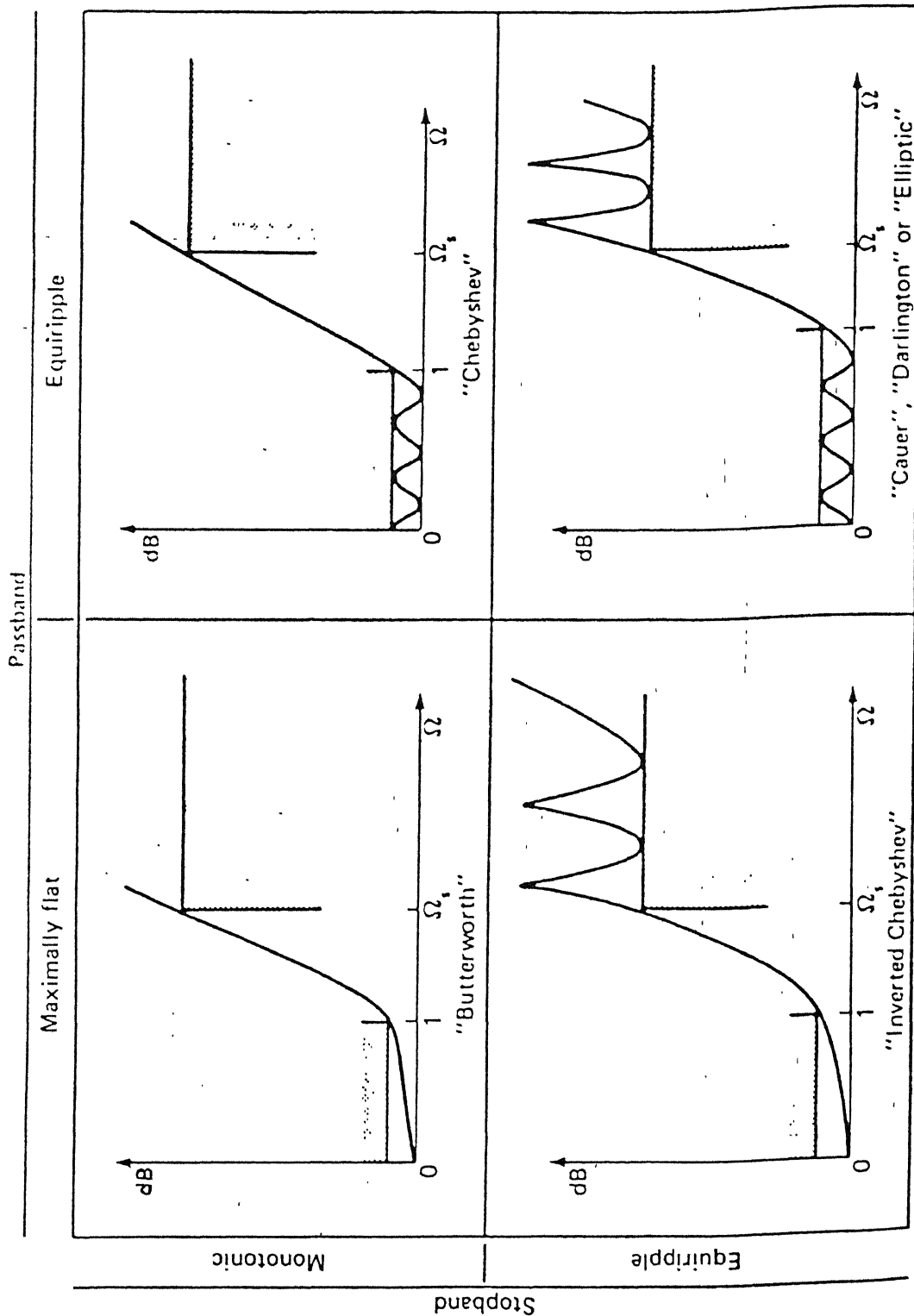


Figure 2.4. The four main classes of approximations.

Now we have to find $\hat{P}(\hat{z})$. It is known that for an elliptic filter, for order n odd, the transfer function has a reflection zero at the origin and a loss pole at ∞ , while for n even, these do not occur. The other reflection zeros and loss poles occur for both cases on the $j\omega$ axis and are all doubled. Thus in the s -plane the characteristic function will be of the form,

$$K(s) = k \frac{s \prod_{i=1}^{(n-1)/2} (s^2 + \Omega_{ri}^2)}{\prod_{i=1}^{(n-1)/2} (s^2 + \Omega_{li}^2)}, \quad n \text{ odd} \quad (2.19a)$$

$$\text{or } K(s) = k \frac{\prod_{i=1}^{n/2} (s^2 + \Omega_{ri}^2)}{\prod_{i=1}^{n/2} (s^2 + \Omega_{li}^2)}, \quad n \text{ even} \quad (2.19b)$$

Then in the \hat{z} plane one can write the squared loss polynomials as

$$\hat{P}(\hat{z}) \hat{P}(-\hat{z}) = (1 - \hat{z}^2) \prod_{i=1}^{(n-1)/2} (\hat{z}^2 - x_i^2)^2, \quad n \text{ odd} \quad (2.20a)$$

$$\text{or } \hat{P}(\hat{z}) \hat{P}(-\hat{z}) = \prod_{i=1}^{n/2} (\hat{z}^2 - x_i^2)^2, \quad n \text{ even} \quad (2.20b)$$

$$\text{where } x_i^2 = 1 - (1 / \Omega_{li}^2) \quad \text{and} \quad 0 < |x_i| < 1 \quad (2.21)$$

The loss poles and reflection zeros exhibit geometrical symmetry around a frequency in the transition band given by $\sqrt{\Omega_s}$. That is

$$\Omega_{l1} \Omega_{r1} = \Omega_{l2} \Omega_{r2} = \dots = \Omega_s \quad (2.22)$$

Now we will present an iterative algorithm [12] that has been followed to get an elliptic low pass prototype filter transfer function :

(1) Find an initial guess for the loss poles $\Omega_{l1}, \Omega_{l2}, \dots$. This can be obtained from applying (2.22) to the reflection zeros (Ω_{ri} 's) of a Chebyshev filter of the same order. These are given by

$$\Omega_{ri} = \cos \left[\frac{2i+1}{n} \cdot \frac{\pi}{2} \right], \quad i = 0, 1, 2, \dots, \frac{n-3}{2} \quad \text{for } n \text{ odd} \quad (2.23a)$$

$$\text{or } i = 0, 1, 2, \dots, \frac{n}{2} - 1 \quad \text{for } n \text{ even} \quad (2.23b)$$

Now we have to find $\hat{P}(\hat{z})$. It is known that for an elliptic filter, for order n odd, the transfer function has a reflection zero at the origin and a loss pole at ∞ , while for n even, these do not occur. The other reflection zeros and loss poles occur for both cases on the $j\omega$ axis and are all doubled. Thus in the s -plane the characteristic function will be of the form,

$$K(s) = k \frac{s \prod_{i=1}^{(n-1)/2} (s^2 + \Omega_{ri}^2)}{\prod_{i=1}^{(n-1)/2} (s^2 + \Omega_{li}^2)}, \quad n \text{ odd} \quad (2.19a)$$

$$\text{or } K(s) = k \frac{\prod_{i=1}^{n/2} (s^2 + \Omega_{ri}^2)}{\prod_{i=1}^{n/2} (s^2 + \Omega_{li}^2)}, \quad n \text{ even} \quad (2.19b)$$

Then in the \hat{z} plane one can write the squared loss polynomials as

$$\hat{P}(\hat{z}) \hat{P}(-\hat{z}) = (1 - \hat{z}^2) \prod_{i=1}^{(n-1)/2} (\hat{z}^2 - x_i^2)^2, \quad n \text{ odd} \quad (2.20a)$$

$$\text{or } \hat{P}(\hat{z}) \hat{P}(-\hat{z}) = \prod_{i=1}^{n/2} (\hat{z}^2 - x_i^2)^2, \quad n \text{ even} \quad (2.20b)$$

$$\text{where } x_i^2 = 1 - (1 / \Omega_{li}^2) \quad \text{and} \quad 0 < |x_i| < 1 \quad (2.21)$$

The loss poles and reflection zeros exhibit geometrical symmetry around a frequency in the transition band given by $\sqrt{\Omega_s}$. That is

$$\Omega_{l1} \Omega_{r1} = \Omega_{l2} \Omega_{r2} = \dots = \Omega_s \quad (2.22)$$

Now we will present an iterative algorithm [12] that has been followed to get an elliptic low pass prototype filter transfer function :

(1) Find an initial guess for the loss poles $\Omega_{l1}, \Omega_{l2}, \dots$. This can be obtained from applying (2.22) to the reflection zeros (Ω_{ri} 's) of a Chebyshev filter of the same order. These are given by

$$\Omega_{ri} = \cos \left[\frac{2i+1}{n} \cdot \frac{\pi}{2} \right], \quad i = 0, 1, 2, \dots, \frac{n-3}{2} \quad \text{for } n \text{ odd} \quad (2.23a)$$

$$\text{or } i = 0, 1, 2, \dots, \frac{n}{2} - 1 \quad \text{for } n \text{ even} \quad (2.23b)$$

- (2) Find x_1, x_2, \dots corresponding to $\Omega_{11}, \Omega_{12}, \dots$ using (2.21).
- (3) Find $\hat{P}(\hat{z}) \hat{P}(-\hat{z})$ from (2.20)
- (4) Find $K(\hat{z})$ from (2.18)
- (5) Get $K(s)$ from $K(\hat{z})$ using the inverse \hat{z}^2 to s^2 mapping (2.16).
- (6) Factor $K(s)$ to obtain new values of Ω_{ri} .
- (7) Apply (2.22) and (2.21) to get new values of Ω_{ri} and x_i .
- (8) Repeat steps (3) to (7) repeatedly unless the process converges to the required accuracy.
- (9) The order n of the filter is calculated by starting with $n = 2$ and repeating steps (1) to (8) and increasing n until

$$As = 10 \log_{10} [1 + |k(j\Omega_s)|^2] \geq \text{the specified } As.$$

- (10) Once $K(s)$ is obtained, Feldtkeller's equation (2.14) is solved to obtain $G(s)$. Then inverting $G(s)$ one gets the required LPP transfer function $H(s)$.

2.3. FREQUENCY TRANSFORMATIONS [10]

In the last section we considered an algorithm to obtain the LPP transfer function. Now we will see how to transform given filter specifications into corresponding LPP specifications and then transform the obtained LPP into the corresponding filter transfer function. Refer to figure 2.5.

(a) Low Pass Filter

The given specifications in this case are As, Ap, fp and fs where $fs > fp$. Then the LPP specifications will be,
 As, Ap , pass band edge $\Omega_p = 1$ and stop band edge $\Omega_s = fs/fp$ in the $\Omega = f/fp$ axis.
 The designed LPP will be normalized with respect to $\omega_p = 2\pi fp$ and thus to obtain LPP transfer function, we have to denormalize the LPP w.r.t ω_p .

(b) High Pass Filter

The given specifications are in this case As, Ap, fp and fs where $fp > fs$. Then the LPP specifications will be,
 As, Ap , pass band edge $\Omega_p = 1$ and stop band edge $\Omega_s = fp/fs$ in the $\Omega = f/fs$ axis.
 The designed LPP will be normalized w.r.t. $\omega_s = 2\pi fs$. Now the lowpass prototype is

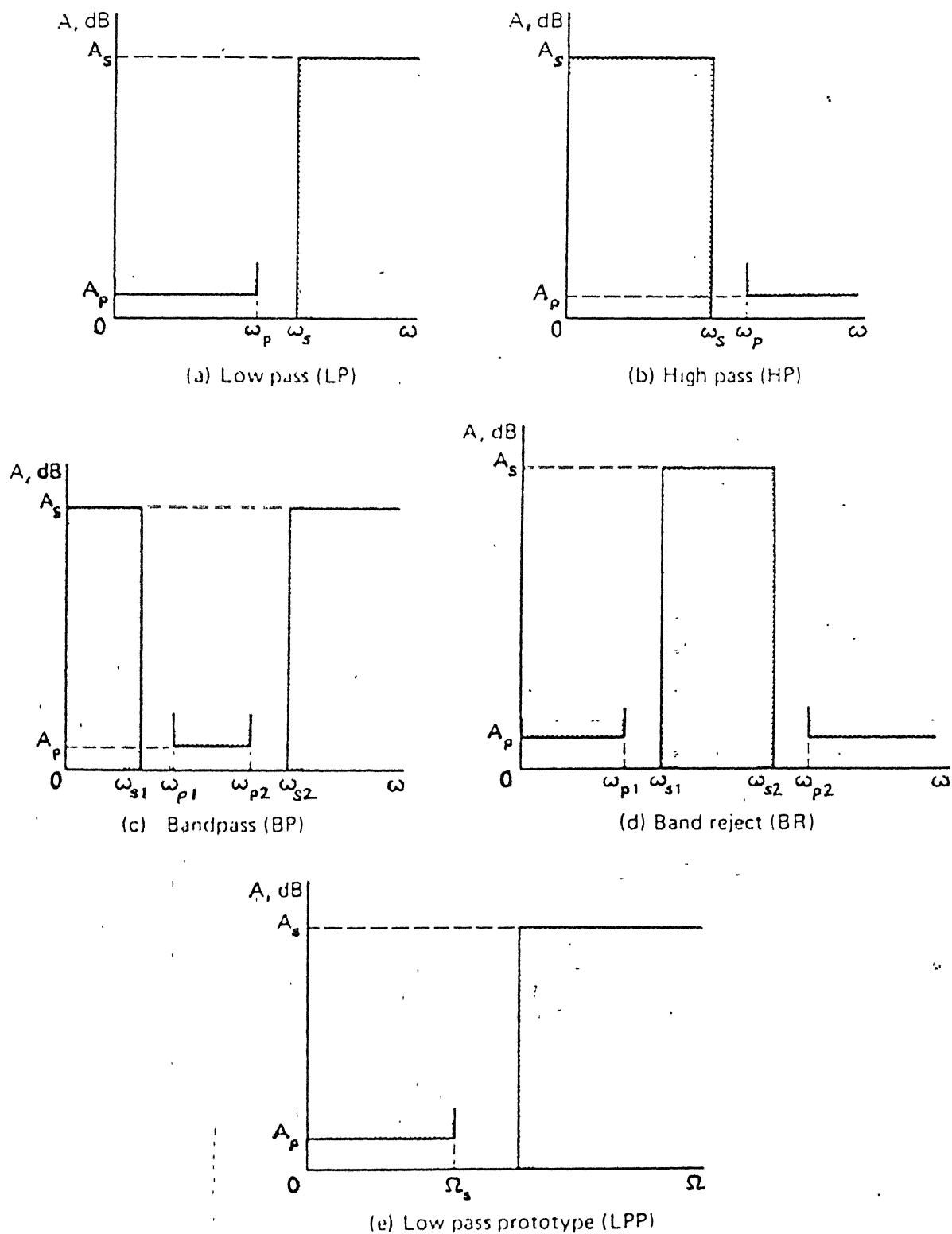


Figure 2.5. Tolerance plots for the various filter types.

transformed into the corresponding high pass prototype (HPP) simply by replacing s by $1/s$ in LPP. Then denormalizing the HPP w.r.t. ω_s one obtains the required HPF transfer function.

(c) Band Pass Filter

The given specifications are

- (1) A_s and A_p
- (2) Lower stopband edge f_{s1}
- (3) Higher stopband edge f_{s2}
- (4) Lower passband edge f_{p1}

and (5) higher passband edge f_{p2} .

To derive the specifications of LPP, the following steps are followed:

- (1) First the center frequency ω_0 is found, which is defined by

$$\omega_0^2 = \omega_{p1} \omega_{p2} \quad \text{where } \omega_{p1} = 2\pi f_{p1} \quad \text{and } \omega_{p2} = 2\pi f_{p2}.$$

- (2) Next we find $\hat{\omega}_{s1} = \omega_0^2 / \omega_{s2}$ where $\omega_{s2} = 2\pi f_{s2}$.

If $\hat{\omega}_{s1}$ is greater than ω_{s1} then we take $\hat{\omega}_{s1}$ and ω_{s2} as the new stopband edges. Otherwise ω_{s1} and $\hat{\omega}_{s2} = \omega_0^2 / \omega_{s1}$ are taken as the new stopband edges. [This is done because the transformations we are considering here are only valid for geometrically symmetric band edges w.r.t. ω_0 , i.e., $\omega_{s1} \omega_{s2} = \omega_0^2$ should hold. Thus step (2) takes care of this without modifying the given specifications in an adverse way. This is so because the new found ω_{s1} or ω_{s2} falls in the transition band only, making the filter characteristics sharper.]

- (3) Thus after obtaining new sets of ω_{s1} and ω_{s2} the LPP specifications are obtained as,

$$A_s, A_p, \text{ pass band edge } \Omega_p = 1 \text{ and stop band edge } \Omega_s = \frac{\omega_{s2} - \omega_{s1}}{\omega_{p2} - \omega_{p1}}$$

With these the LPP is obtained. This LPP is normalized w.r.t. ω_0 . Now one gets the Band Pass Prototype (BPP) transfer function from LPP using the following transformation :

$$s = \frac{p^2 + 1}{kp} \quad \text{where} \quad k = \frac{\omega_{p2} - \omega_{p1}}{\omega_0}$$

This BPP is again normalized w.r.t. ω_0 and hence it is denormalized to obtain the required band pass filter transfer function.

(d) Band Reject Filter

The given specifications are as before

- (1) A_s and A_p
- (2) f_{s1} , f_{s2} , f_{p1} and f_{p2} .

The LPP specifications are obtained similarly as the BPF case:

- (1) ω_0 = center frequency = $\sqrt{(\omega_{s1}\omega_{s2})}$
- (2) ω_{p1} and ω_{p2} are adjusted as in the case of step (2) in BPF.
- (3) LPP specifications are thus

$$A_s, A_p, \text{ pass band edge } \Omega_p = 1 \text{ and stop band edge } \Omega_s = \frac{\omega_{p2} - \omega_{p1}}{\omega_{s2} - \omega_{s1}}$$

The corresponding LPP is then obtained and this is then transformed into a band reject prototype transfer function through the transformation

$$s = \frac{kp}{p^2 + 1} \quad \text{where} \quad k = \frac{\omega_{p2} - \omega_{p1}}{\omega_0}$$

This BRP is again normalized w.r.t. ω_0 and hence is denormalized to get the required band reject filter transfer function.

The above considerations are presented in a tabular form in table 2.1. In the above discussion we did not present the actual equations which have been used to obtain the different transformations mentioned. We will now derive the equation for the BPF case and state the equations for the other cases without deriving them.

Let us consider a LPP transfer function having the form

$$H(s) = \frac{a_0 + a_1s + \dots + a_{m-1}s^{m-1} + a_ms^m}{b_0 + b_1s + \dots + b_{n-1}s^{n-1} + b_ns^n}$$

The LPP to BPP transformation is given by $s = \frac{p^2 + 1}{kp}$. Putting this in $H(s)$ we obtain,

$$\begin{aligned} H(s) &= \frac{a_0 + a_1\left(\frac{p^2 + 1}{kp}\right) + a_2\left(\frac{p^2 + 1}{kp}\right)^2 + \dots + a_m\left(\frac{p^2 + 1}{kp}\right)^m}{b_0 + b_1\left(\frac{p^2 + 1}{kp}\right) + b_2\left(\frac{p^2 + 1}{kp}\right)^2 + \dots + b_n\left(\frac{p^2 + 1}{kp}\right)^n} \\ &= (kp)^{n-m} \frac{a_0 (kp)^m + a_1(kp)^{m-1} (p^2 + 1) + \dots + a_m (p^2 + 1)^m}{b_0 (kp)^n + b_1(kp)^{n-1} (p^2 + 1) + \dots + b_n (p^2 + 1)^n} \end{aligned}$$

Type	Direction of Transformation	Transformation	Notes
LP	LP \rightarrow LPP	$\Omega_s = \frac{\omega_s}{\omega_p}$	
	LPP \rightarrow LP	$s = \frac{p}{\omega_p}$	
HP	HP \rightarrow LPP	$\Omega_s = \frac{\omega_p}{\omega_s}$	
	LPP \rightarrow HP	$s = \frac{\omega_p}{p}$	
BP	BP \rightarrow LPP	$\Omega_s = \frac{\omega_{s2} - \omega_{s1}}{\omega_{p2} - \omega_{p1}}$	$\omega_o^2 = \omega_{p1} \omega_{p2} = \omega_{s1} \omega_{s2}$ $B = \omega_{p2} - \omega_{p1}$
	LPP \rightarrow BP	$s = \frac{p^2 + \omega_o^2}{pB}$	
BR	BR \rightarrow LPP	$\Omega_s = \frac{\omega_{p2} - \omega_{p1}}{\omega_{s2} - \omega_{s1}}$	Same as above
	LPP \rightarrow BR	$s = \frac{pB}{p^2 + \omega_o^2}$	

TABLE 2.1. FREQUENCY-BAND TRANSFORMATIONS

$$= (kp)^{n-m} \frac{\sum_{i=0}^m a_i (kp)^{m-i} (p^2 + 1)^i}{\sum_{i=0}^n a_i (kp)^{n-i} (p^2 + 1)^i}$$

Now as $(p^2 + 1)^i = \sum_{j=0}^i {}^iC_j p^{2j}$ we get

$$H(p) = (kp)^{n-m} \left(\frac{\sum_{i=0}^m \sum_{j=0}^i {}^iC_j k^{m-i} p^{m-i+2j}}{\sum_{i=0}^n \sum_{j=0}^i {}^iC_j k^{n-i} p^{n-i+2j}} \right) \quad (2.24)$$

Thus, LPP to BPP transformation is obtain through equation (2.24). One can similarly show that LPP to HPP transformation [$s = 1/p$] is given by

$$H(p) = p^{n-m} \left(\frac{\sum_{i=0}^m a_i p^{m-i}}{\sum_{i=0}^n b_i p^{n-i}} \right) \quad (2.25)$$

and LPP to BRP transformation [$s = kp / (p^2 + 1)$] is given by

$$H(p) = \left(\frac{\sum_{i=0}^m \sum_{j=0}^{n-i} a_i {}^{n-i}C_j k^i p^{m-i+2j}}{\sum_{i=0}^n \sum_{j=0}^{n-i} b_i {}^{n-i}C_j k^i p^{i+2j}} \right) \quad \text{for } n > m \quad (2.26)$$

When a given $H(s)$ is to be denormalized w.r.t. ω_c , the transformation is given by $p = s\omega_c$. Thus the transformation equation will be

$$H(p) = \left(\frac{\sum_{i=0}^m a_i \omega_c^i p^i}{\sum_{i=0}^n b_i \omega_c^i p^i} \right) \quad (2.27)$$

2.4 CASCADE FILTER

So far we have seen how to derive a transfer function that meets the given specifications for all major types of filter specifications, i.e., BP, LP, HP and BR types. Now we will see how this transfer function, which is the ratio of two polynomials of order m and n in general, can be broken up into product of biquadratic blocks to be designed separately and then joined to produce a cascade filter. The idea is shown schematically in fig. 2.6.

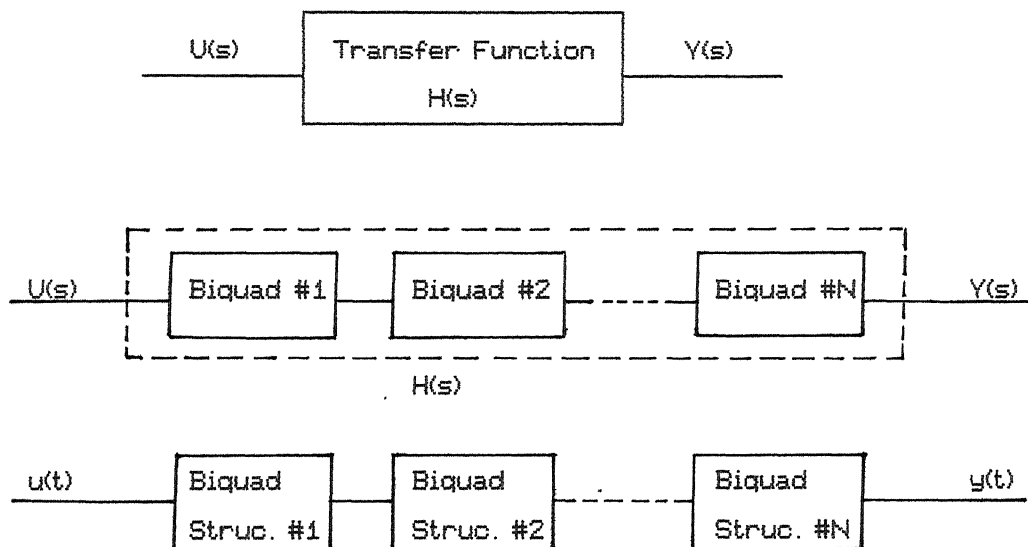


Figure 2.6. Realization of Cascade Filters

Note that cascade filter design give exact overall transfer function because of the fact that the output of each biquad is from an operational amplifier output node, which being a low impedance node eliminates any possibility of feedbacks.

Mathematically the decomposition problem can be stated as follows: given an n th order transfer function $H(s)$, we have to decompose it into product of second order (and one first order, for n odd) subfunctions; that is

$$H(s) = \prod_{j=1}^{n/2} H_j(s), \quad n \text{ even where } H_j(s) \text{ has the general form}$$

$$H_j(s) = K_j \frac{s^2 + s \left(\frac{\omega_{zj}}{Q_{zj}} \right) + \omega_{zj}^2}{s^2 + s \left(\frac{\omega_{oj}}{Q_j} \right) + \omega_{oj}^2} \quad (2.28)$$

where ω_{oj} is the frequency and Q_j is the Q factor of the jth natural mode or pole. This problem can be split into two parts:

(1) Pole Zero Pairing : To form second order functions, each of the $(n/2)$ pole-pairs has to be combined with one of the $(n/2)$ pairs of zeros (including those at $s=0$ and $s=\infty$). There are $(n/2)!$ possible different combinations to choose from.

(2) Cascading sequence : Having determined the transfer function of each filter section, to within a gain constant, one has to choose the sequence in which the sections are to be cascaded. There are $(n/2)!$ possible sequences to choose from.

It turns out that, among many filter performance measures which one may attempt to optimize in solving the decomposition problem, the dynamic range is by far the most relevant, as this is affected the most. In order to obtain the widest possible dynamic range, two objectives have to be met. These are:

(1) Solve the pairing problem such that the magnitude of the transfer function of each biquad is as flat as possible over the filter passband.

(2) Find the sequence of cascading the biquads (obtained as a result of step (1)) such that the magnitude of the intermediate transfer functions is as flat as possible over the filter passband.

The pole-zero pairing as above can be done as follows:

$$\text{We define from (2.8) } F_j(\omega) = |H_j(j\omega) / K_j|^2 \quad (2.29)$$

$$\text{We define } F_{j\max} = \text{Max} [F_j(\omega)], \quad 0 \leq \omega \leq \infty \quad (2.30)$$

$$\text{and } F_{j\min} = \text{Min} [F_j(\omega)], \quad \omega_l \leq \omega \leq \omega_h \quad (2.31)$$

where ω_l = lower passband edge and ω_h = higher passband edge.

$$\text{Then we define } d_j = \log \left(F_{j\max} / F_{j\min} \right) \quad (2.32)$$

which is a logarithmic measure of flatness. Our attempt will be to keep such d_j 's as low as possible. The pole-zero pairing algorithm can then be stated as follows:

(1) For a possible pole-zero arrangement, find the values of d_j , $j=1,2,\dots,n/2$.

Find the maximum value of d for this assignment,

$$d_{\max} = \text{Max} [d_j], \quad j = 1,2,3,\dots,n/2.$$

(2) Repeat step (1) for every possible pole-zero assignments. The optimum

assignment is the one having the smallest d_{\max} .

To find optimum sequence we proceed as follows:

Let $H_j(j\omega)$ be the cascaded sequence at present after the optimum pole-zero pairing.

Then we form

$$d_1 = \log \frac{\text{Max } |H_1(j\omega)|}{\text{Min } |H_1(j\omega)|}$$

$$d_2 = \log \frac{\text{Max } |H_1(j\omega) H_2(j\omega)|}{\text{Min } |H_1(j\omega) H_2(j\omega)|}$$

.....

$$d_{n-1} = \log \frac{\text{Max } |H_1(j\omega) \dots H_{n-1}(j\omega)|}{\text{Min } |H_1(j\omega) \dots H_{n-1}(j\omega)|}$$

where for evaluating maxima we use $0 \leq \omega \leq \infty$ and for minima $\omega_l \leq \omega \leq \omega_h$. Then we find $d_{\max} = \text{Max } [d_j, j=1, 2, 3, \dots, n-1]$. This is done for all possible sequences. The sequence with the lowest d_{\max} is chosen.

Thus we have been able to obtain a cascaded sequence from the given specifications. In the next chapter we will consider how these blocks can be implemented using switched capacitor circuits, a special type of sampled data analog circuits.

CHAPTER 3

SWITCHED CAPACITOR FILTER

In this chapter we will consider the design of *Switched Capacitor (SC) Filters*. Firstly, the *z transform* will be briefly discussed, as SC circuits are designed in the *z* domain. Then SC circuits will be discussed in general followed by *cascade* SC filter design. In the last section we will discuss about the different non linear effects which influence SC filter performance.

3.1 SAMPLING AND THE *z* TRANSFORM

Switched capacitor circuits are *sampled data analog circuits*. That is, the input signals are sampled at a certain clock rate before any processing is done. The sampled signals are not digitized as in a fully digital system, but the analog sampled signals are processed. The the SC circuits fall in between a fully analog and a fully digital system.

As SC circuits operate in discrete time, analysis of such circuits are done using the *z transform* [13]. Let $f(t)$ be an input signal and let $f(t)$ be sampled at time $t = 0, T, 2T, \dots$. Then the unilateral *z* transform of such a pulse train is defined as

$$F(z) = \sum_{n=0}^{\infty} f(nT) z^{-n} \quad (3.1)$$

Note that the *z* transform is only related to the samples $f(nT)$ of $f(t)$; it is independent of the function values between the samples. The mapping between the *s* plane (Laplace transform domain) and the *z* plane is given by

$$z = e^{sT} \quad (3.2)$$

where T is as before the sampling time period. The left half *s* plane gets mapped into a *unit disk* with center at the origin in the *z* plane. Thus for stability, the poles of the transfer function in the *z* domain must lie within the unit disk.

The spectrum of a sampled signal is obtained by replacing z by $e^{j\omega T}$ in (3.1). Then

$$F^*(j\omega) = \sum_{n=0}^{\infty} f(nT) e^{-jn\omega T} \quad (3.3)$$

The relation between the Fourier transform $F(j\omega)$ of the analog signal and the spectrum of the sampled signal $F^*(j\omega)$ is given by

$$F^*(j\omega) = \sum_{k=-\infty}^{\infty} F(j\omega - jk\frac{2\pi}{T}) \quad (3.4)$$

From (3.3) we get that $F^*(j\omega)$ is a periodic function of ω with a period of $2\pi/T$. The sampling frequency should be greater than twice the maximum signal frequency (the *Nyquist rate*) to avoid *aliasing or folding*.

The SC filters that we will consider are *Infinite Impulse Response (IIR)* filters having a transfer function of the form

$$H(z) = \frac{N(z)}{D(z)} = \frac{a_0 + a_1z + a_2z^2 + \dots + a_mz^m}{b_0 + b_1z + b_2z^2 + \dots + b_nz^n} \quad (3.6)$$

Our strategy is to use the s domain transfer functions already derived in chapter 2. This can be done by using some rational function of the form $s = f(z)$ to transform an s domain transfer function $H(s)$ into a z domain transfer function of the form (3.6). There are several such functions which approximate the exact transform $z = e^{sT}$. We will use the bilinear s to z transformation [13] given by

$$s = \frac{2}{T} \frac{z - 1}{z + 1} \quad (3.7)$$

Let us consider a general filter transfer function in the s domain

$$H(s) = \frac{a_0 + a_1s + a_2s^2 + \dots + a_ms^m}{b_0 + b_1s + b_2s^2 + \dots + b_ns^n} \quad (3.8)$$

Then one can derive the equation to transform $H(s)$ into $H(z)$ using the bilinear s to z transformation, viz.,

$$H(z) = \frac{\sum_{i=0}^m \sum_{j=0}^i \sum_{k=0}^{n-i} a_i k^i (-1)^{i-j} i_{C_j} n-i_{C_k} z^{j+k}}{\sum_{i=0}^n \sum_{j=0}^i \sum_{k=0}^{n-i} b_i k^i (-1)^{i-j} i_{C_j} n-i_{C_k} z^{j+k}} \quad (3.9)$$

where $k = 2/T$ and $n \geq m$.

The relation between ω_a , the analog signal frequency and ω , the corresponding transformed frequency is given by

$$\omega_a = \frac{2}{T} \tan \left(\frac{\omega T}{2} \right) \text{ or, equivalently, } \omega = \frac{2}{T} \tan^{-1} \left(\frac{\omega_a T}{2} \right) \quad (3.10)$$

This relation is shown pictorially below in figure (3.1).

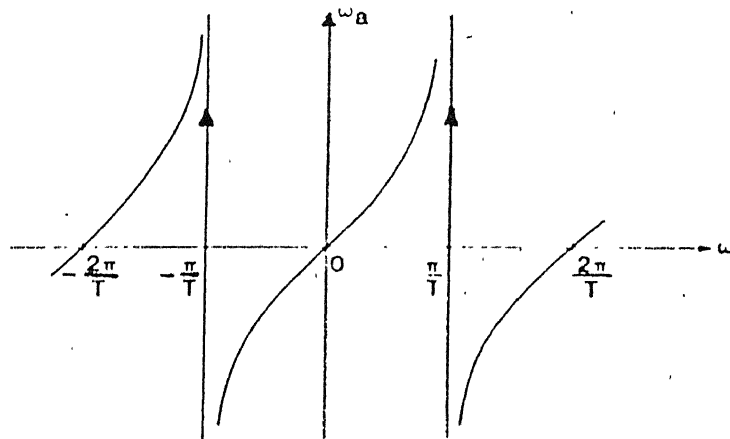


Figure 3.1. The relation between the continuous time and sampled data frequencies for the bilinear s to z mapping.

As seen, the frequency scale of ω axis is *warped* as compared to that of the ω_a axis. To counter this nonlinearity, the specifications for a corresponding continuous time filter must be *prewarped*. Thus, instead of ω_p and ω_s , the model must be designed for the band limited frequencies

$$\omega_{ap} = \frac{2}{T} \tan \left(\frac{\omega_p T}{2} \right) \quad (3.11a)$$

$$\omega_{as} = \frac{2}{T} \tan \left(\frac{\omega_s T}{2} \right) \quad (3.11b)$$

Thus one synthesizes a continuous time s domain transfer function as in Chapter 2 using ω_{ap} and ω_{as} instead of ω_p and ω_s and then one can use equation (3.9) to obtain $H(z)$.

3.2 SWITCHED CAPACITOR CIRCUITS [4],[14],[15]

In chapter 1 we introduced SC circuits as a special type of sampled data circuits which use only capacitors, op-amps and switches. The most important aspect of these circuits is to simulate a resistance using capacitances and switches, which makes high level of integration possible. While analyzing the SC circuit in chapter 1, the treatment was somewhat heuristic. A detailed analysis of an SC integrator is presented now.

Consider figure 3.2 which shows an RC integrator and a corresponding SC integrator which uses the resistor simulation circuit described above. In the figure clocks ϕ_1 and ϕ_2 are shown as logic variables operating between 0 and 1. The transfer function of the integrator of fig. 3.2a is given by

$$H_a(s_a) = \frac{V_o(s_a)}{V_{in}(s_a)} = - \frac{1/RC}{s_a} \quad (3.12)$$

where s_a is the analog Laplace transform variable. When ϕ_1 rises to 1 at $t = t_n - \tau$, M_1 turns on and C_1 (which was earlier discharged) recharges to v_{in} . At $t = t_n$, M_1 shuts off and C_1 having acquired a charge

$$\Delta q_1(t_n) = C_1 v_{in}(t_n) \quad (3.13)$$

is isolated. At $t = t_n + T/2 - \tau$, ϕ_2 rises to 1 and M_2 turns on. Thus C_1 is connected between the virtual ground at the inverting input of the op-amp and hence it discharges. Thus a charge

$$\Delta q_2(t_n + T/2 - \tau) = C_1 v_{in}(t_n) \quad (3.14)$$

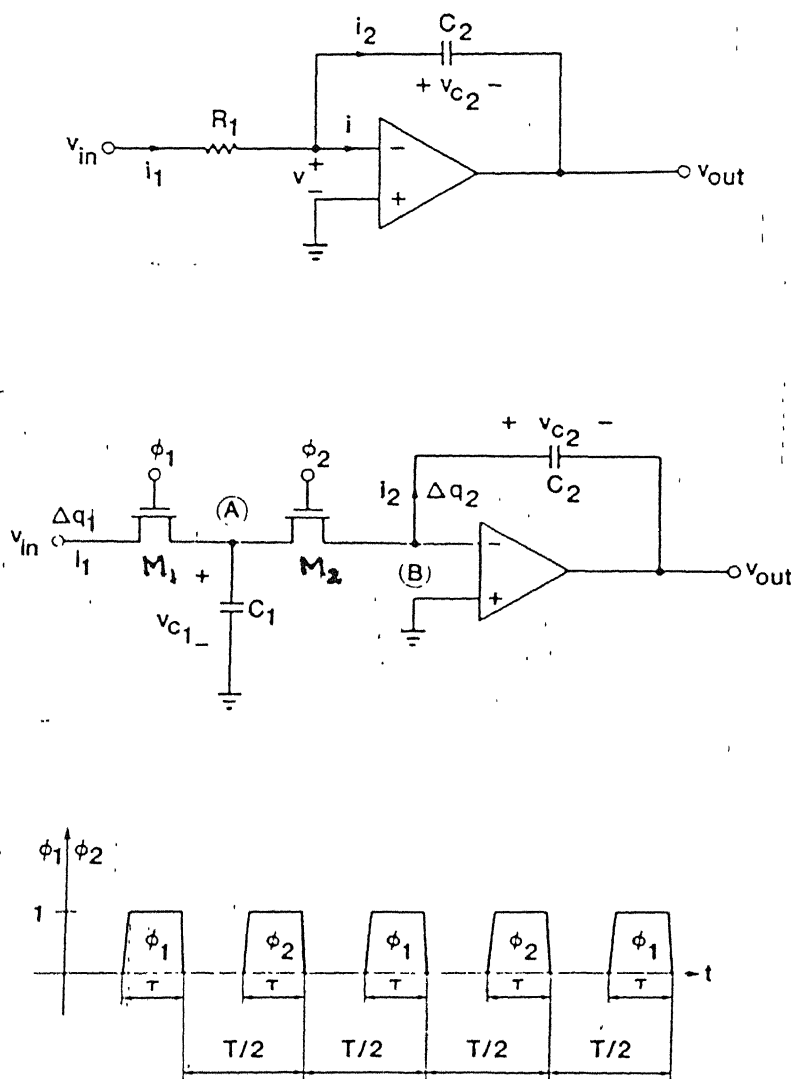


Figure 3.2. Shunt Switched capacitor integrator realization: (a) active RC circuit; (b) SC realization; (c) clock signals.

flows through M_2 and into C_2 . As a result, the charge stored in C_2 increases by Δq_2 , and the voltage v_{o2} across it changes by

$$\Delta v_{o2}(t_n + T/2 - \tau) = \left(\frac{C_1}{C_2} \right) v_{in}(t_n) \quad (3.15)$$

We can form a difference equation between the samples of $v_{in}(t)$ and $v_o(t)$ taken at t_{n-1} , t_n , t_{n+1} and so on.

$$v_o(t_{n+1}) - v_o(t_n) = - \left(\frac{C_1}{C_2} \right) v_{in}(t_n) \quad (3.16)$$

Using z transform we get,

$$H(z) = \frac{v_o(z)}{v_{in}(z)} = - \left(\frac{C_1}{C_2} \right) \frac{z^{-1}}{1 - z^{-1}} \quad (3.17)$$

Other types of switching arrangements give rise to other types of transformations.

The SC circuit described above is sensitive to the effects of *stray capacitances* between the various nodes and ground. To eliminate the harmful effects of stray capacitors, the circuit [16] shown in figure (3.3) can be used. The circuit has a transfer function similar to equation (3.17). In this circuit, the stray capacitance C_A between node (A) and ground is periodically charged from the input source which provides v_{in} and then is discharged to ground. C_B (which loads node (B)) is grounded at both terminals, as is C_C . Finally, C_D is driven by the low-impedance output of the op-amp, and is hence rendered harmless. In the present work, such stray insensitive circuits are used throughout.

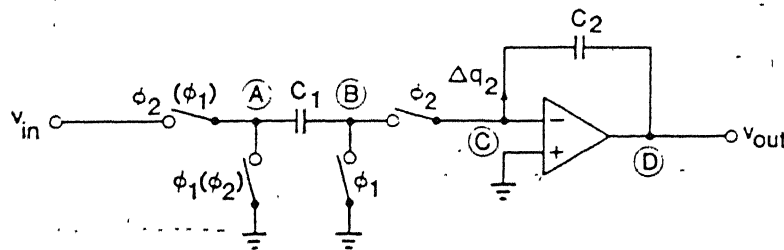


Figure 3.3. Stray insensitive integrator.

3.3 CASCADE FILTER DESIGN [14]

Using the SC integrator blocks, it is possible to construct simple filter sections. For cascade filter design, we use the biquads as mentioned in chapter 2. Such a transfer function in the z domain is of the form

$$H(z) = - \frac{a_0 + a_1 z + a_2 z^2}{1 + b_1 z + b_2 z^2} \quad (3.18)$$

To obtain an SC biquad structure and get the coefficient values a_i and b_i in equation (3.18) we proceed as follows.

A biquad transfer function in the s domain can be written as

$$H_a(s) = \frac{V_O(s)}{V_{in}(s)} = - \frac{k_0 + k_1 s + k_2 s^2}{\omega_0^2 + (\frac{\omega_0}{Q}) s + s^2} \quad (3.19)$$

This can be rewritten as

$$V_O = - (1/s) [(k_1 + k_2 s) V_{in} + (\omega_0/Q) V_O - \omega_0 V_1] \quad (3.20)$$

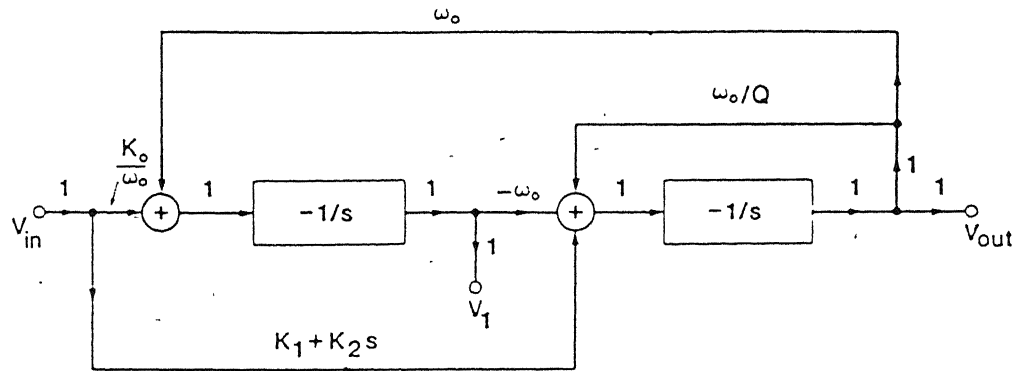
$$\text{where } V_1 = - (1/s) \left(\frac{k_0}{\omega_0} V_{in} + \omega_0 V_O \right) \quad (3.21)$$

Note that equation (3.19) can be partitioned differently giving rise to different filter structure.

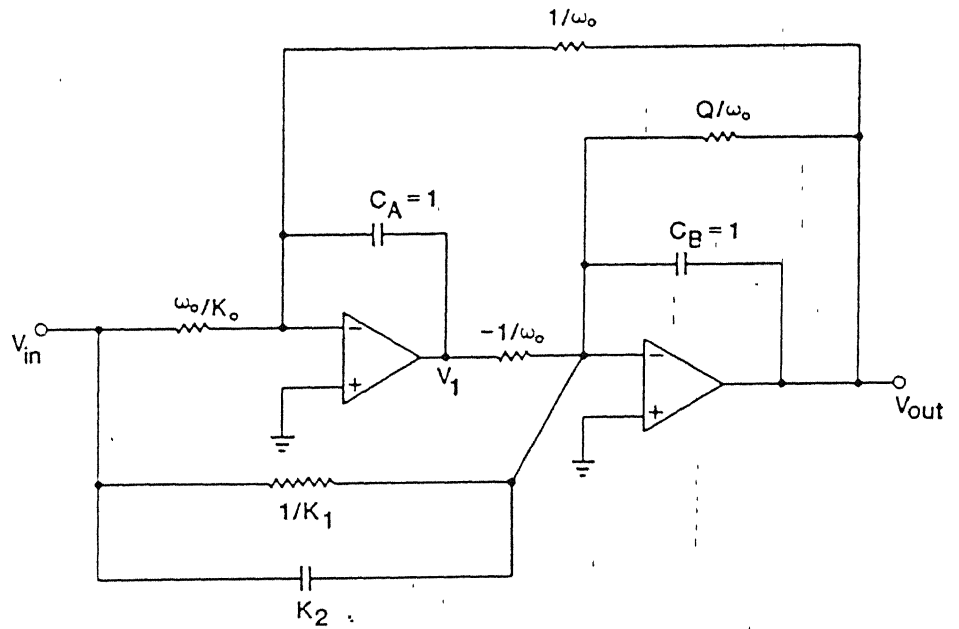
An active RC filter can be realized from these equations as shown in figure 3.4a and 3.4b. Then by replacing the resistances by stray insensitive circuits described earlier, one gets the SC biquad (figure 3.4c). Now one would like to get the exact transfer function of this SC biquad in the z domain. This can be obtain as follows :

Let us denote, as before, the charge flowing into an integrator during the n th clock period $(n-1)T \leq t \leq nT$ by $\Delta q(t_n)$ and the value of a voltage at $t=nT$ by $v(t_n)$. Let the corresponding z transforms be $\Delta Q(z)$ and $V(z)$ respectively. Then for an integrator (containing an op-amp and its feedback capacitor C), the transfer function is obtained from

$$v_{out}(t_n) - v_{out}(t_{n-1}) = - (1/C) \Delta q_{in}(t_n)$$

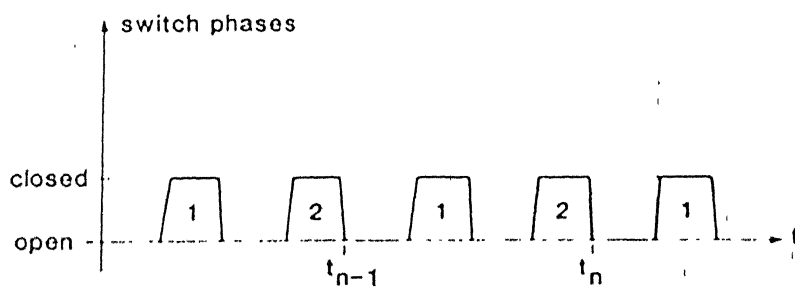
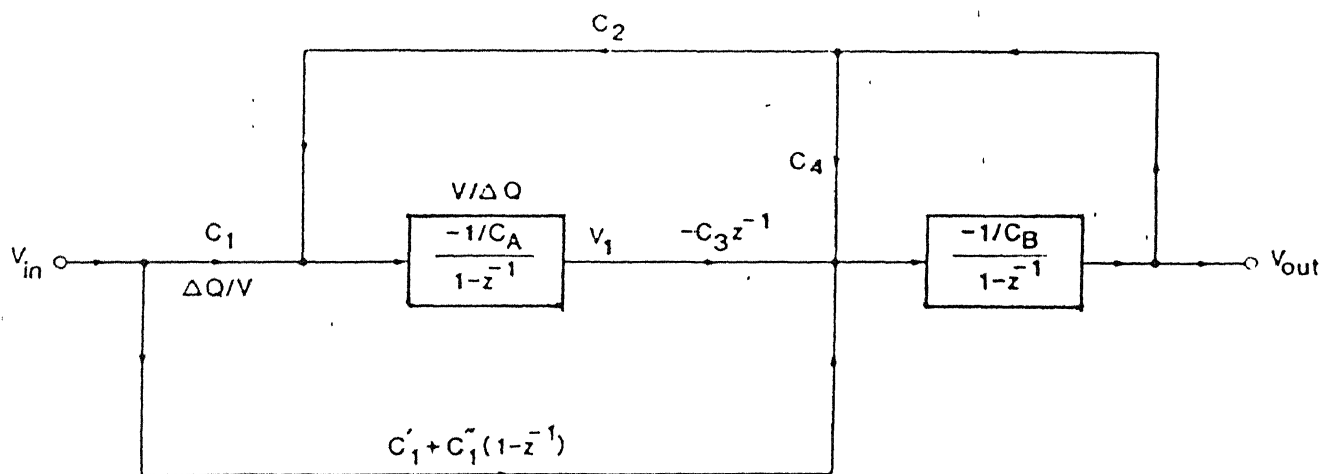
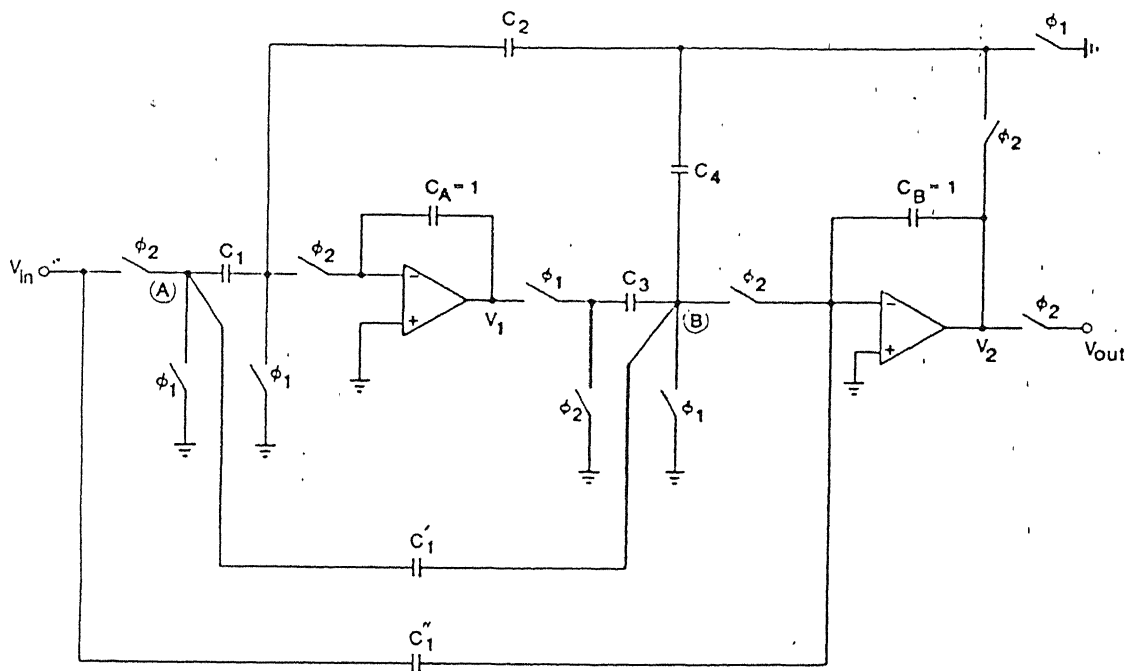


(a)



(b)

Figure 3.4. Switched capacitor low-Q biquad: (a) block diagram in the s-domain; (b) active RC realization; (c) SC circuit; (d) block diagram in the z-domain.



$$\text{giving } H(z) = \frac{V_{\text{out}}(z)}{\Delta Q_{\text{in}}(z)} = - \frac{1/C}{1 - z^{-1}} \quad (3.22)$$

Similar transfer functions (but defined by the ratio $\Delta Q_{\text{out}}/V_{\text{in}}$) can be derived for the coupling branches. Assuming that V_{in} changes only as ϕ_2 goes high, one obtains

$$H(z) = \frac{\Delta Q}{V} = \begin{cases} C(1 - z^{-1}) & \text{for an unswitched capacitor} \\ C & \text{for a non inverting switched capacitor} \\ -C z^{-1} & \text{for an inverting switched capacitor} \end{cases} \quad (3.23)$$

Using these transfer functions a block diagram as shown in figure 3.4d can be obtained, which is exactly equivalent to the circuit of fig. 3.4c. Then we get,

$$\begin{aligned} H(z) &= \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} \\ &= - \frac{C_A(C_1' + C_1'')z^2 + (C_1C_3 - C_AC_1' - 2C_AC_1'')z + C_AC_1''}{C_A(C_B + C_4)z^2 + (C_2C_3 - C_AC_4 - 2C_AC_B)z + C_AC_B} \end{aligned} \quad (3.24)$$

Thus, an exact realization of $H(z)$ given in equation (3.18) is done by matching the coefficients of the two rational functions in z . This gives, as $C_A = C_B = 1$,

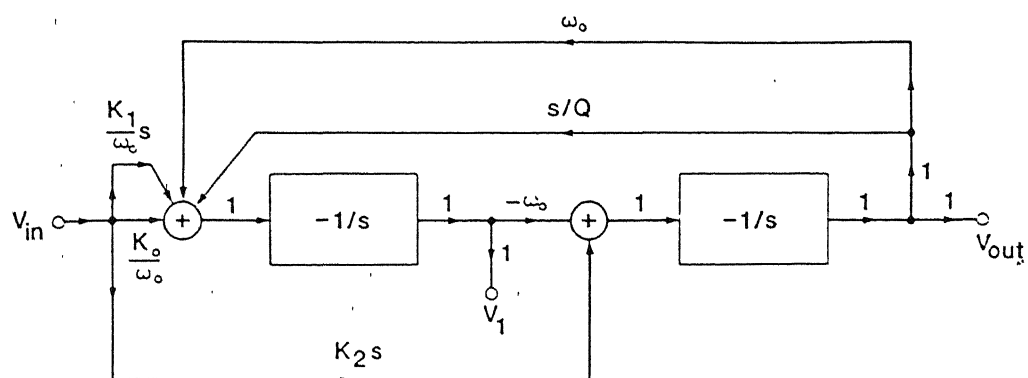
$$\begin{aligned} a_0 &= C_1'' ; \quad C_1' = a_2 - a_0 ; \quad C_1 = (a_0 + a_1 + a_2) / C_3 ; \\ C_4 &= b_2 - 1 ; \quad C_2 C_3 = b_1 + b_2 + 1 ; \end{aligned} \quad (3.25)$$

One important consideration for such SC biquads is the capacitance spread, defined as $C_{\text{max}}/C_{\text{min}}$, where C_{max} and C_{min} are the maximum and minimum capacitances in the circuit respectively. It is desirable to keep this value to the minimum. For $Q \leq 1$,

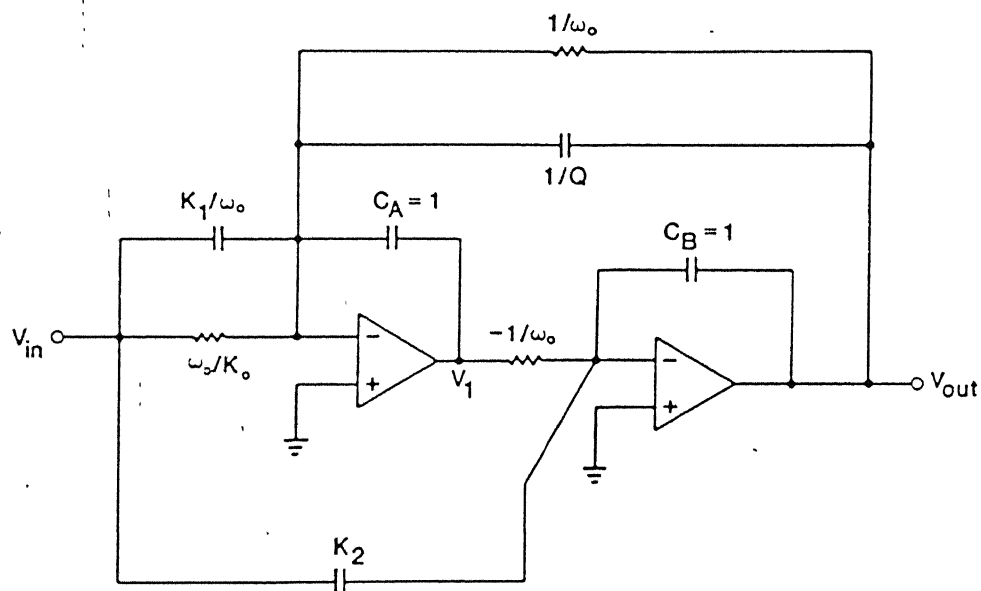
$$C_{\text{max}}/C_{\text{min}} = C_A/C_2 \simeq 1/(\omega_0 T), \text{ where } \omega_0 \text{ is the pole frequency.}$$

But for $Q > 1$, $C_4 < \omega_0 T$ and spread equals $\frac{C_A}{C_4} = \frac{Q}{\omega_0 T} > \frac{1}{\omega_0 T}$. Thus, this

circuit is suitable for low Q pole realization only. For high Q section, we use the circuit shown in figure 3.5c. The realization is done as shown in fig. 3.5. The partition of equation 3.18 is done differently in this case,

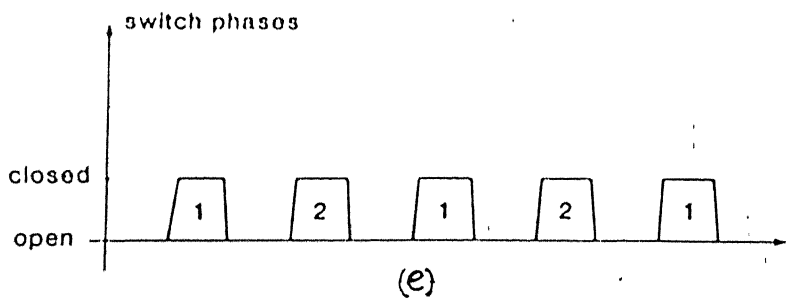
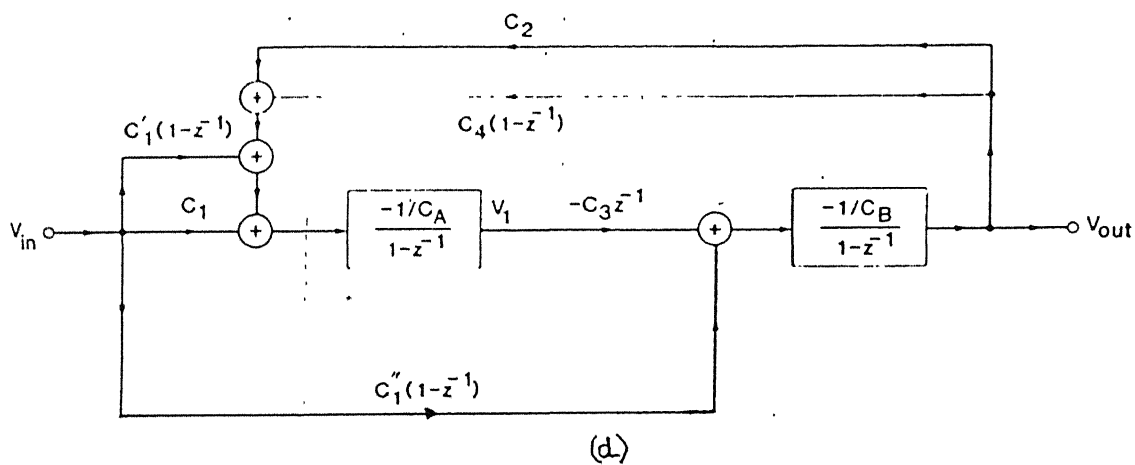
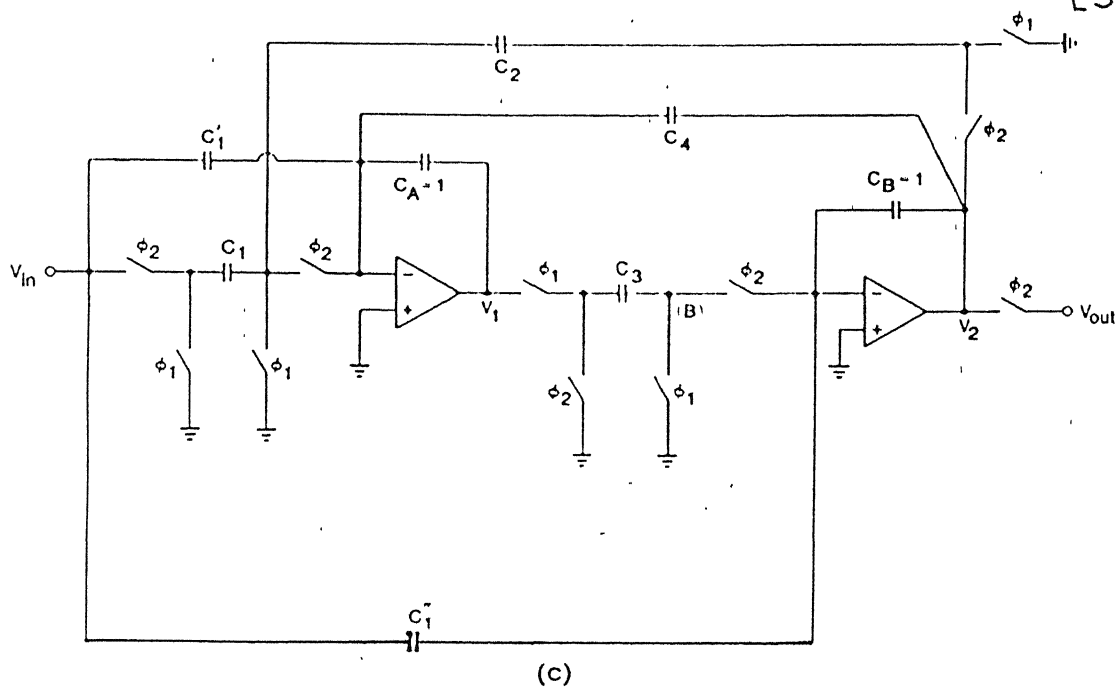


(a)



(b)

Figure 3.5. Switched capacitor high-Q biquad: (a) block diagram in the s-domain; (b) active RC realization; (c) SC circuit; (d) block diagram in the z-domain.



$$V_{out} = - (1/s) (k_2 s V_{in} - \omega_0 V_1) \quad (3.26)$$

$$\text{where } V_1 = - (1/s) \left(\left(\frac{k_0}{\omega_0} + \frac{k_1}{\omega_0} \right) V_{in} + \left(\omega_0 + \frac{s}{Q} \right) V_{out} \right) \quad (3.27)$$

From the z domain block diagram of figure 3.5d, one gets,

$$\begin{aligned} H(z) &= \frac{V_{out}(z)}{V_{in}(z)} \\ &= - \frac{C_A C_1'' z^2 + (C_1 C_3 + C_3 C_1' - 2C_A C_1'')z + (C_A C_1'' - C_3 C_1')}{C_A C_B z^2 + (C_2 C_3 + C_3 C_4 - 2C_A C_B)z + (C_A C_B - C_3 C_4)} \end{aligned} \quad (3.28)$$

Comparing with equation (3.18)

$$\begin{aligned} C_1'' &= \frac{a_2}{b_2} ; \quad C_1' = \frac{a_2 - a_0}{b_2 C_3} ; \quad C_1 = (a_0 + a_1 + a_2) / (b_2 C_3) ; \\ C_4 &= (1 - 1/b_2) / C_3 ; \quad C_2 C_3 = (b_1 + b_2 + 1) / C_3 ; \end{aligned} \quad (3.29)$$

If the order of $H(z)$, obtained by bilinear transform of $H(s)$ obtained in chapter 2 is odd, then one needs linear sections of the form

$$H(z) = - \frac{a_0 + a_1 z}{1 + b_1 z} \quad (3.30)$$

This can be realized as shown in figure 3.6. The exact transfer function is given by,

$$H(z) = - \frac{(C_1 + C_1') z - C_1}{(1 + C_2) - 1} \quad (3.31)$$

comparing with (3.30) we get

$$C_1 = -a_0 ; \quad C_1' = a_0 + a_1 ; \quad C_2 = b_2 - 1 ; \quad (3.32)$$

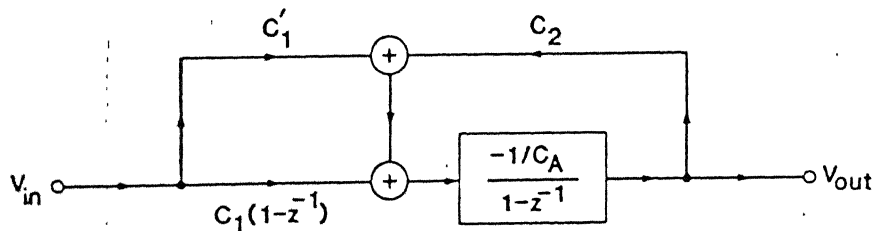
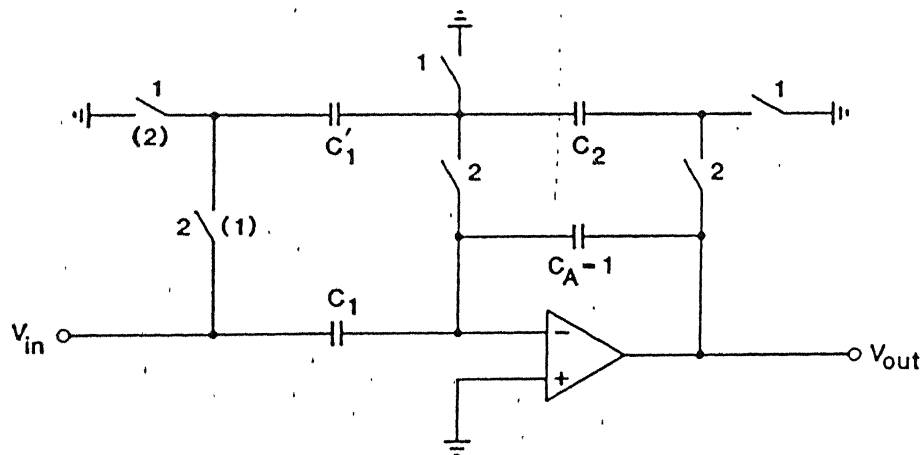
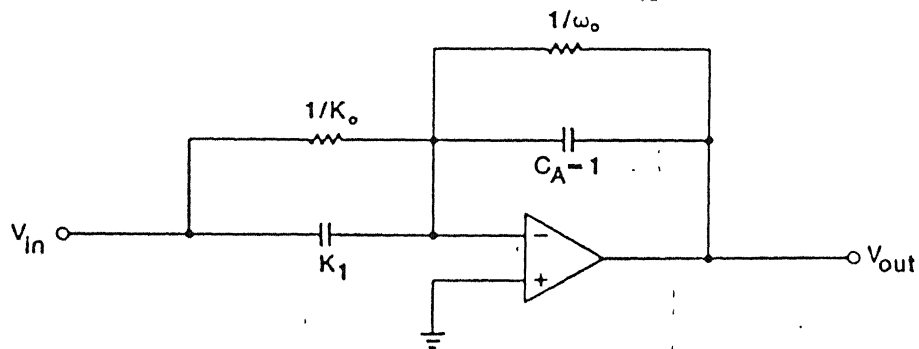
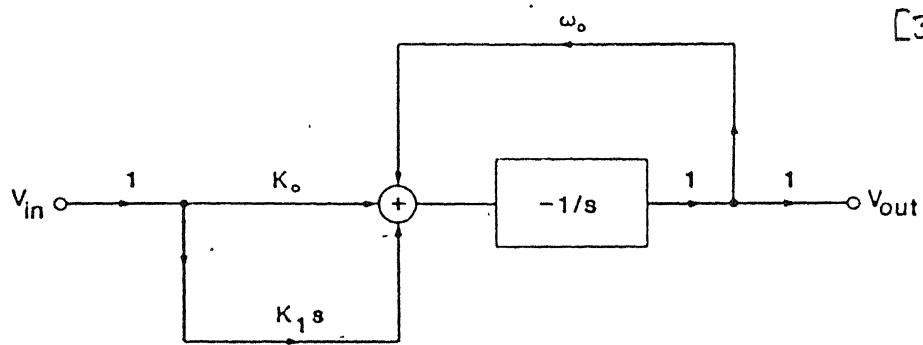


Figure 3.6. Switched capacitor linear section: (a) block diagram in the s-domain; (b) active RC realization; (c) SC circuit; (d) block diagram in the z-domain.

3.4 SCALING OF SWITCHED CAPACITOR FILTERS [17],[18]

The actual performance of SCF can be improved, and the area which it occupies on its silicon chip reduced, by scaling operation. To understand how such operations can be carried out, let us consider a segment of an SCF containing the i th op-amp OA_i and all the branches connected to it, as shown in figure (3.7).

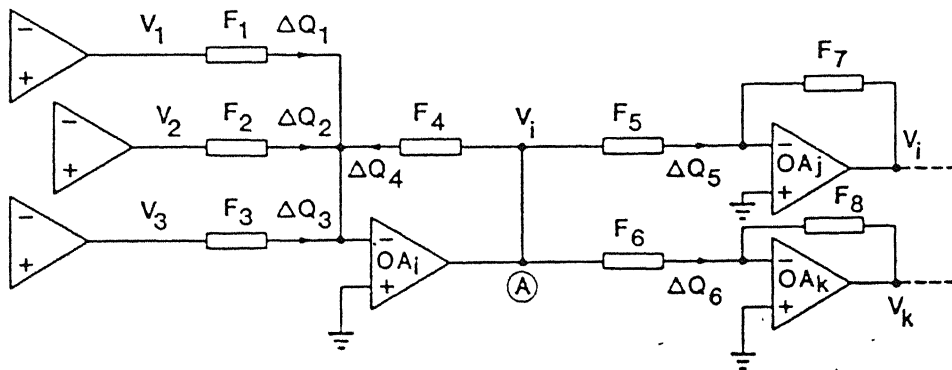


Figure 3.7. An SC filter section.

In this figure the coupling branches may contain capacitors and switches in any arrangements. Each of these can be described, as in equation (3.23) by a transfer function of the form $F_k(z) = \Delta Q_k(z)/V_1(z)$. Now let all the branches connected to the output terminal of OA_i be modified such that their $\Delta Q/V$ transfer functions (F_4 , F_6 , F_8) are multiplied by a positive real constant factor k_i . This can be achieved by multiplying all capacitances in these branches by k_i , since their charges are proportional to these capacitances. Since the input branches and their voltages are kept unchanged, the charge flowing in the feedback branch remains at its original value. The output voltage OA_i thus becomes

$$\hat{V}_i(z) = \Delta Q_4(z) / [k_i F_4(z)] = V_i(z) / k_i$$

Thus V_i gets transformed to V_i / k_i . By contrast, the values of ΔQ_5 and ΔQ_6 remain unchanged.

Thus we have seen that multiplying all capacitances which are connected (

or switched) to the output terminal of the i th op-amp OA_i changes its output voltage V_i to V_i/k_i , while leaving all charges flowing from (and to) OA_i to (and from) the rest of the circuit unchanged. By this operation we can increase or decrease V_i by a constant scale factor without affecting any other voltages or charges in the SCF.

This operation is useful in improving the dynamic range $[20 \log_{10}(V_{in,max}/V_{in,min})]$ of SC circuits. But output noise grows with increasing k_i , the scaling factor, although the rate of increase is slower than linear. By scaling, the semilogarithmic and logarithmic sensitivities of an SCF, defined by

$$\begin{aligned} \frac{\partial V_{out}}{\partial (\ln C_r)} &= C_r \frac{\partial V_{out}}{\partial C_r} \\ \frac{\partial (\ln V_{out})}{\partial (\ln C_r)} &= \frac{C_r}{V_{out}} \frac{\partial V_{out}}{\partial C_r} \end{aligned} \quad (3.33)$$

remains unchanged. It can be shown that for maximum dynamic range, all op-amp outputs should be scaled such that each (at its own maximum frequency) saturates for the same input voltage level.

Another form of scaling is to scale the capacitances connected to the input of an op-amp OA_i . This does not affect the output voltage, which remains unchanged. This scaling reduces the capacitance spread and the total capacitance of an SCF. One can thus normalize an SCF w.r.t. the minimum capacitance.

When scaling is performed, scaling for maximum dynamic range is performed first followed by scaling for minimum capacitance. The steps that are followed are [14] :

1. Scaling for maximum dynamic range

- (a) Set $v_{in}(\omega)$ to the largest value for which the output op-amps do not saturate.
- (b) Calculate the maximum values V_{pi} for all internal op-amp output voltages.
- (c) Multiply all capacitances connected or switched to the output terminal of op-amp i by $k_i = V_{pi}/V_{i,max}$, where $V_{i,max}$ is the saturation voltage of op-amp i .

(d) Repeat for all internal op-amps.

2. Scaling for minimum capacitance

- (a) Divide all capacitors in an SCF into non overlapping sets. Capacitors in the i th set S_i are connected or switched to the input terminal of op-amp i .
- (b) Multiply all capacitors in S_i by $m_i = C_{\min}/C_{i,\min}$, where C_{\min} is the smallest capacitor which the fabrication technology permits, and $C_{i,\min}$ is the smallest capacitor in S_i .
- (c) Repeat for all sets S_i , including that associated with the output op-amp.

3.5 NON IDEAL EFFECTS IN SC CIRCUITS [19],[20]

In this section we will consider some nonideal effects which influence the performance of switched capacitor circuits.

(a) Nonideal Effects in the Switches

Consider the MOS switch in figure (3.8a). As shown, the stray capacitances C_{gs} and C_{gd} provide feedback paths between gate and source and gate and drain. Thus the clock V_ϕ applied at the gate is fed back to nodes (1) and (2) and the signals v_1 and v_2 will contain a *clock feedthrough* noise. This can be countered if one uses a *transmission gate* as shown in figure (3.8b). Here as the two clocks are compliments of each other, a feedback cancellation results.

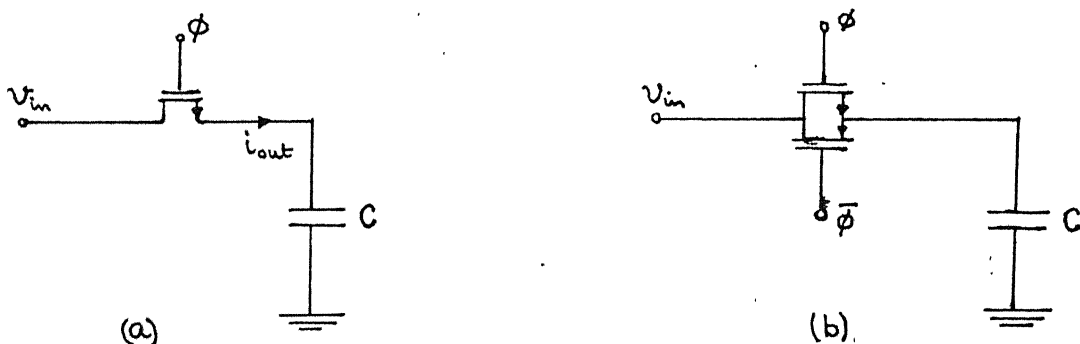


Figure 3.8. (a) NMOS transistor used as a switch, (b) CMOS transmission gate.

The MOS switches also suffer from *nonzero on resistance*. As the clock signal is usually the supply voltage (V_{DD} or V_{SS}), normally $|v_{GS} - V_T| > |v_{DS}|$ and the transistors are in the linear region. Thus the on resistance is approximately,

$$R_{on} = \frac{1}{2k(v_{GS} - V_T)} \quad (3.34)$$

In a typical application, the switch is used to charge a capacitance as shown in figure (3.8a). Due to this on resistance, a nonzero charging time is required for this operation. Also, when v_{in} nears V_{DD} , the signal gets *clipped* as the MOS nears saturation. All these effects are reduced when a transmission gate is used. Also it can be shown that the effect of on resistance is to reduce the value of the capacitance ratios C_1/C_2 of a circuit. For better operation a value of $RC_{max} \leq T/2$ should be chosen.

(b) Non Ideal OP-AMP Circuit Effects

Due to the finite dc gain of an op-amp, the capacitance ratios of the form C_1/C_2 get deviated from their nominal values. The relative error is of the order of $1/A_O$. Normally, for a gain of more than 1000, this effect is negligible. Due to the finite unity-gain bandwidth of op-amps, the transfer function of the filter gets modified. To minimize this effect, the *unity-gain bandwidth* ω_O of the op-amps used should be at least five times as large as the clock frequencies. Also, to avoid distortions, the slew rate of the op-amps S_r should be $\geq 20\omega_B V_{max}$ where ω_B is the baseband frequency of the filter and V_{max} is the largest voltage swing of the op-amp.

(c) Noise Generated In SC Circuits

The internally generated noise in an SC circuit consists of the *flicker and thermal noises*. Due to the internal sampling and holding performed by the switches and capacitors this noise will be replicated in the frequency domain. For usual parameter values, this does not lead to appreciable aliasing of the $1/f$ noise; since the corner frequency f_{cr} is usually well below $f_C/2$; however, the thermal noise will get seriously undersampled and hence aliased. As a result of the aliasing, the power spectral density of the low frequency thermal noise will be multiplied by $2f_{noise}/f_C$, where f_{noise} is the bandwidth of the thermal noise after being band limited by the circuit. The noise bandwidth is determined by the time

constants of the on resistance of the switches multiplied by the switched capacitances, and by the op-amp bandwidths. Hence, to minimize noise aliasing, these time constants should be as large and the op-amp bandwidths should be as low as possible. Typically, $R_{on}C \simeq 0.1mT$ and $\omega_0 \simeq 5\omega_c$ may be used. All noise effects, along with the clock feedthrough noise, are reduced if the circuit capacitances are increased; the noise power being proportional to $1/C_{min}$.

CHAPTER 4

OPERATIONAL AMPLIFIERS

In the previous chapter we have seen that *operational amplifier* (op-amp) [21] is an essential building block for switched capacitor filter design. We will, in this chapter, discuss how to design such op-amps. Our focus will be on CMOS op-amps, which have been used in the designed filters.

4.1 PRACTICAL CONSIDERATIONS [14]

Ideally operational amplifier is a voltage controlled voltage source with infinite voltage gain and with zero input admittance as well as zero output impedance. It is free of temperature dependence, distortion and noise. Needless to say, practical op-amps can only approximate such an ideal device. The main differences between the ideal op-amp and the real devices are the following:

- (1) *Finite Gain*: For practical op-amps, the voltage gain is finite. Typical values for low frequencies and small signals range from $A = 10^2$ to 10^5 , corresponding to 40 to 100 dB gain.
- (2) *Finite Linear Range*: The linear relation $v_o = A(v_a - v_b)$ between the input and output voltages is valid only for a limited range of v_o . Normally, the maximum value of v_o for linear operation is somewhat smaller than the positive dc supply voltage; the minimum value of v_o is somewhat positive with respect to the negative supply.
- (3) *Offset Voltage*: For an ideal op-amp, if $v_a = v_b$ then $v_o = 0$. In real devices this is not true and a voltage $v_{o,off} \neq 0$ will occur at the output for shorted inputs. This can also be described in terms of input offset voltage, which is directly proportional to output. Typical values of $v_{in,off}$ is about 5 - 15 mV.
- (4) *Common Mode Rejection Ratio (CMRR)*: The common mode input voltage is defined by $v_{in,c} = (v_a + v_b) / 2$ as contrasted with the differential-mode input voltage $v_{in,d} = (v_a - v_b)$. Accordingly, we can define the differential gain A_d and also the common-mode gain A_c where $A_d = v_o / v_{in,d}$ and $A_c = v_o / v_{in,c}$.

The CMRR is now defined as A_D / A_C or in logarithmic units $CMRR = 20 \log_{10}(A_D / A_C)$ in dB. Typical values for MOS op-amps range between 60 to 80 dB. The CMRR measures how much the op-amp can suppress common-mode signals at its inputs.

- (5) *Frequency Response*: Because of stray capacitances, finite carrier mobility etc., the gain A decreases at high frequency. The effect is described in terms of unity gain bandwidth, that is the frequency f_D at which $|A(f_D)| = 1$. For MOS op-amps this is of the order of 1 to 10 MHz.
- (6) *Slew Rate*: For a large input step voltage, some transistors in the op-amp may be driven out of their saturation regions or completely cut off. As a result the output will follow the input at a slower finite rate. The maximum rate of change dv_O/dt is called the slew rate. Typical values range between 1 to 20 V/ μ s.
- (7) *Noise*: MOS transistors generate noise, which can be described in terms of an equivalent current source in parallel with the channel of the device. The noisy transistors in an op-amp give rise to a noise voltage v_{on} at the output of the op-amp; this can be also modelled by an equivalent voltage source $v_n = v_{on}/A$ at the op-amp input. In a wide band (say, in the 10Hz to 1 MHz range), the equivalent input noise source is usually of the order of 10 - 50 μ V RMS.
- (8) *Dynamic Range*: Due to the limited linear range of an op-amp, there is a maximum input signal $v_{in,max}$ which the device can handle without generating an excessive amount of nonlinear distortion. Due to spurious signals (noise, clock feedthrough, crossover distortion etc.) there is also a minimum input signal $v_{in,min}$ which still does not drown in noise and distortion. The dynamic range of an op-amp is then defined as $20 \log_{10}(v_{in,max} / v_{in,min})$. Typical values are 80 - 90 dB for switched capacitor circuits.
- (9) *Power Supply Rejection Ratio (PSRR)*: If a power supply voltage contains an incremental component v due to noise, hum, etc., then a corresponding voltage $A_P v$ will appear at the op-amp output. The PSRR is defined as A_D/A_P , where $A_D = A$ is the differential gain. Typical values are 30-50 dB.
- (10) *DC power dissipation*: Typical values are 0.25 - 10 mW.

The op-amps are designed so as to minimize these effects.

4.2 BASIC BUILDING BLOCKS [22]

The following figure shows the basic building blocks of an op-amp.

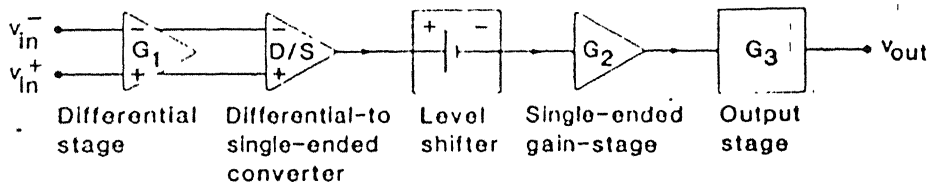


Figure 4.1. Basic building blocks of an operational amplifier.

We will now discuss how to design some of these building blocks. First we consider how to realize voltage and current sources, which are required to realize the above shown building blocks.

VOLTAGE AND CURRENT SOURCES

Many circuit configurations are possible for realizing a voltage source. We present here some circuits which have been used in the design. Consider figure (4.2). From the figure, $V_{bias} = V_{GS2} + V_{SS}$ and $V_{GS1} = -V_{bias}$. Thus one can find the W and L values of $M1$ and $M2$ as,

$$\left(\frac{W}{L} \right)_1 = \frac{I_b}{k_n' (V_{GS1} - V_{TN})^2} \quad (4.1a)$$

$$\left(\frac{W}{L} \right)_2 = \frac{I_b}{k_n' (V_{GS2} - V_{TN})^2} \quad (4.1b)$$

V_D and I_b are insensitive to variations of V_{DD} , but not to changes in V_{SS} . If V_{SS}

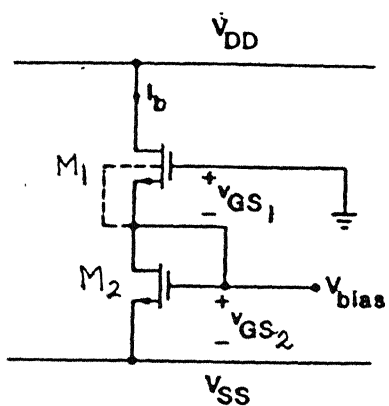


FIGURE 4.2. VOLTAGE SOURCE

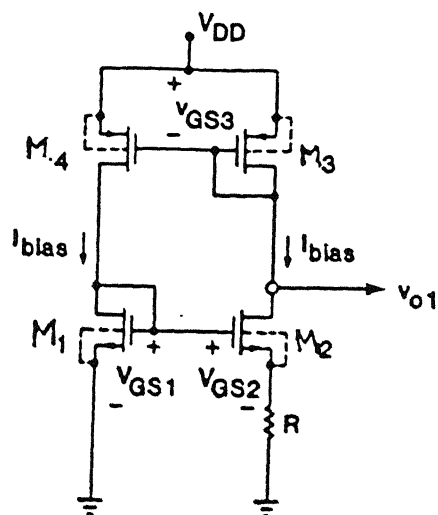
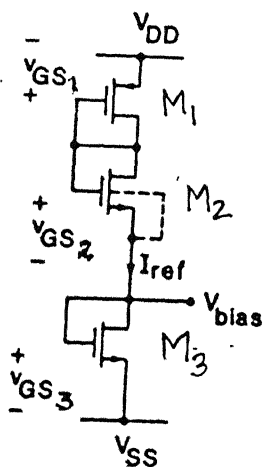
FIGURE 4.3. SUPPLY INDEPENDENT
VOLTAGE BIAS CIRCUIT.

FIGURE 4.4. A BIAS CIRCUIT.

changes to $V_{SS} + \Delta V_{SS}$, one gets,

$$V_{GS2}' = \frac{V_{TN} (\sqrt{(k_2/k_1)} - 1) - V_{SS} - \Delta V_{SS}}{\sqrt{(k_2/k_1)} + 1} \quad (4.2)$$

$$V_{GS1}' + V_{GS2}' = -V_{SS} - \Delta V_{SS} \quad \text{and} \quad I_D' = k_2 (V_{GS2}' - V_{TN})^2$$

where prime denotes changed value.

If the variations are not acceptable one may use the supply independent bias circuit shown in figure (4.3). Here M3 and M4 are matched transistors, i.e., $(W/L)_3 = (W/L)_4$. Then,

$$I_{bias} = (V_{GS1} - V_{GS2}) / R = \left[\frac{1}{R^2 k'} \right] \left[\left(\frac{W}{L} \right)_1^{-\frac{1}{2}} - \left(\frac{W}{L} \right)_2^{-\frac{1}{2}} \right]^2 \quad (4.3)$$

Sometimes supply independent biasing may cause problem and then one may use the circuit shown in figure (4.4).

One can easily form a current source by biasing a transistor in its saturation region using above discussed bias circuits and using the drain currents for driving other circuits. One can find a large variety of such circuits in reference [14].

DIFFERENTIAL INPUT STAGE

The input stage of an op-amp must provide a high input impedance, large common mode rejection ratio (CMRR), large power supply rejection ratio (PSRR), low dc offset voltage, low noise and much (or all) of the op-amps voltage gain. The circuit shown in figure (4.5a) has a differential input and single-ended output. Thus it is a combination of the first two stages of the block diagram of figure (4.1). The circuit is analyzed as below:

In the analysis we assume that the transistors M1 and M2 are identical. Also we assume that M1 and M2 are in saturation. The small signal equivalent circuit is shown in figure (4.5b). Applying KCL to the nodes (a), (b) and (c) we get,

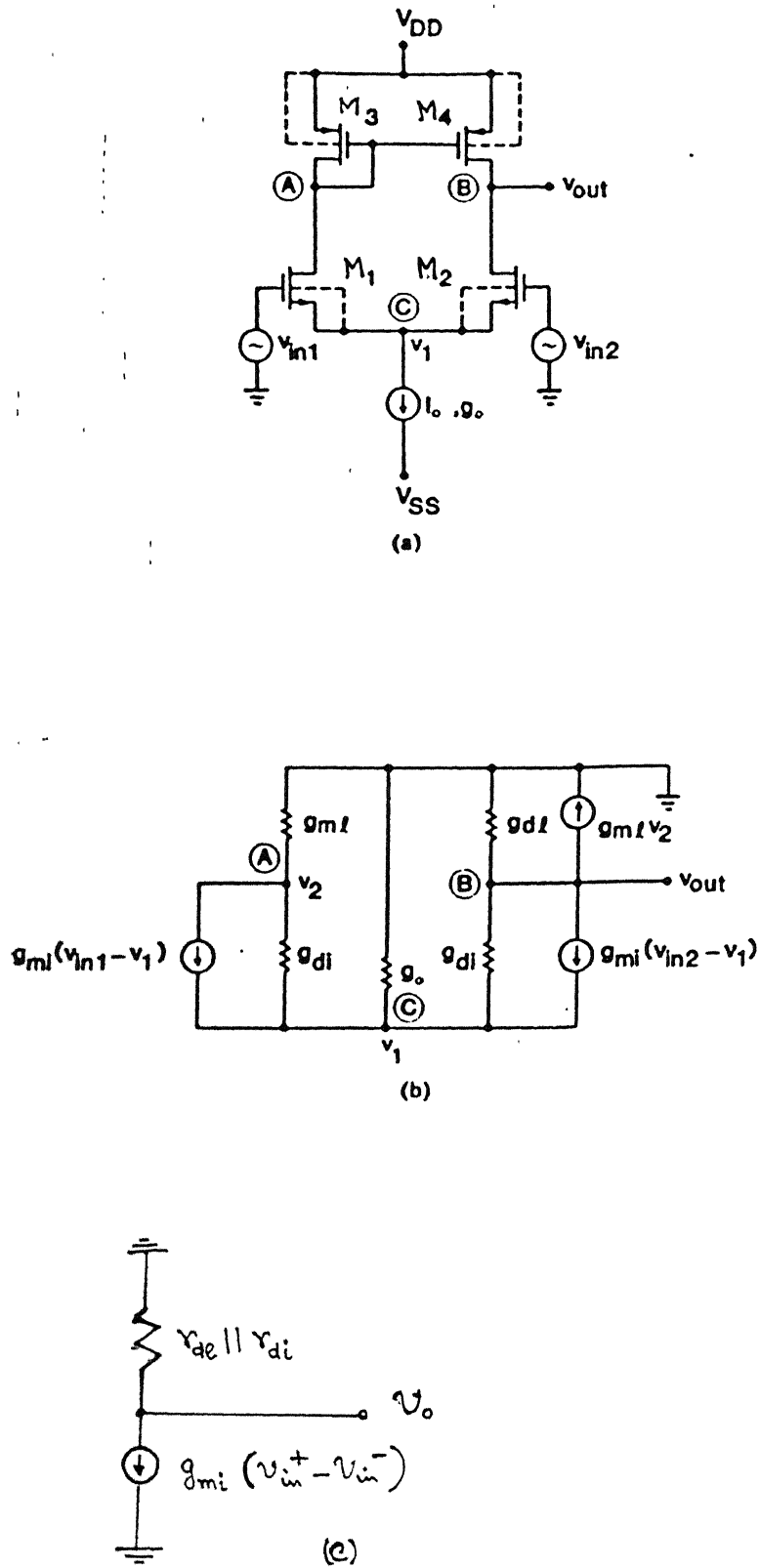


Figure 4.5. (a) Differential input stage, (b) small signal equivalent circuit, (c) approximate equivalent circuit.

$$v_2 g_{m1} + (v_2 - v_1) g_{di} + g_{mi} (v_{in1} - v_1) = 0 \quad (4.4)$$

$$v_o g_{d1} + (v_o - v_1) g_{di} + g_{m1} v_2 + g_{mi} (v_{in2} - v_1) = 0 \quad (4.5)$$

$$v_1 g_o + (v_1 - v_2) g_{di} + (v_1 - v_o) g_{di} - g_{mi} (v_{in1} - v_1) - g_{mi} (v_{in2} - v_1) = 0 \quad (4.6)$$

Using these equations and noting that

$$v_o = A_{dm} (v_{in1} - v_{in2}) + A_{cm} \left(\frac{v_{in1} + v_{in2}}{2} \right) \quad (4.7)$$

we get,

$$A_{dm} = \frac{g_{mi} g_{m1}}{D} [2 (g_{di} + g_{mi}) + g_o (1 + \frac{g_{di}}{2g_{m1}})] \quad (4.8)$$

$$\text{and } A_{cm} = -g_{mi} g_{di} g_o / D \quad (4.9)$$

where

$$D = g_{di} (g_{di} + g_{mi})(2g_{di} + g_{d1}) - (g_{di} + g_{d1})(g_{di} + g_{m1})(g_o + 2g_{di} + 2g_{mi})$$

Then,

$$\text{CMRR} = \left| \frac{A_{dm}}{A_{cm}} \right| = \frac{g_{m1}}{g_o g_{d1}} [2(g_{m1} + g_{di}) + g_o] + \frac{1}{2} \quad (4.10)$$

For $g_{m1}, g_{m1} \gg g_o, g_{di}, g_{d1}$, one may have the approximate expressions,

$$A_{dm} \approx g_{mi} / (g_{d1} + g_{di}) \quad (4.11)$$

$$A_{cm} \approx -\frac{g_o g_{d1}}{2g_{m1}(g_{d1} + g_{di})} \quad (4.12)$$

$$\text{and } \text{CMRR} \approx 2 \frac{g_{mi} g_{m1}}{g_o g_{d1}} \quad (4.13)$$

Small signal output impedance of the stage is approximately

$$r_o \approx 1 / (g_{d1} + g_{di}) \quad (4.14)$$

An approximate equivalent circuit is shown in figure (4.5c).

4.3 COMPLETE OP-AMP CIRCUITS [22]

Consider the circuit diagram of a two stage CMOS op-amp shown in figure (4.6a). M1, M2, M3 and M4 form the differential input stage as discussed above. M9, M10, M5 and M7 provide the current sources. M6 and M7 combination is the source follower output buffer. M8 and C_0 are for (internal) frequency compensation. For zero output offset voltage, the condition is that for zero input voltage, the output current should be zero. That is,

$$I_6 = I_7 - I_8 \quad \text{and} \quad V_O = 0 \quad (4.15)$$

$$\text{now,} \quad I_6 = 2 k' \left(\frac{W}{L} \right)_6 (|V_{SS}| - V_{TP}) (V_{DD} - V_{GS6}) \quad (4.16)$$

From (4.15) and (4.16) we can get zero offset condition, when all other voltages and currents are known.

To reduce random offset voltage, it can be shown that one has to reduce I_O or increase $(W/L)_1$ and thus g_{m1} . Both reduces $V_{GS1} - V_{T1}$.

The slew rate is given by

$$S_r = \left| \frac{dv_O}{dt} \right| = \left| - \frac{1}{C_O} \frac{dQ_O}{dt} \right| = \frac{I_O}{C_O} \quad (4.17)$$

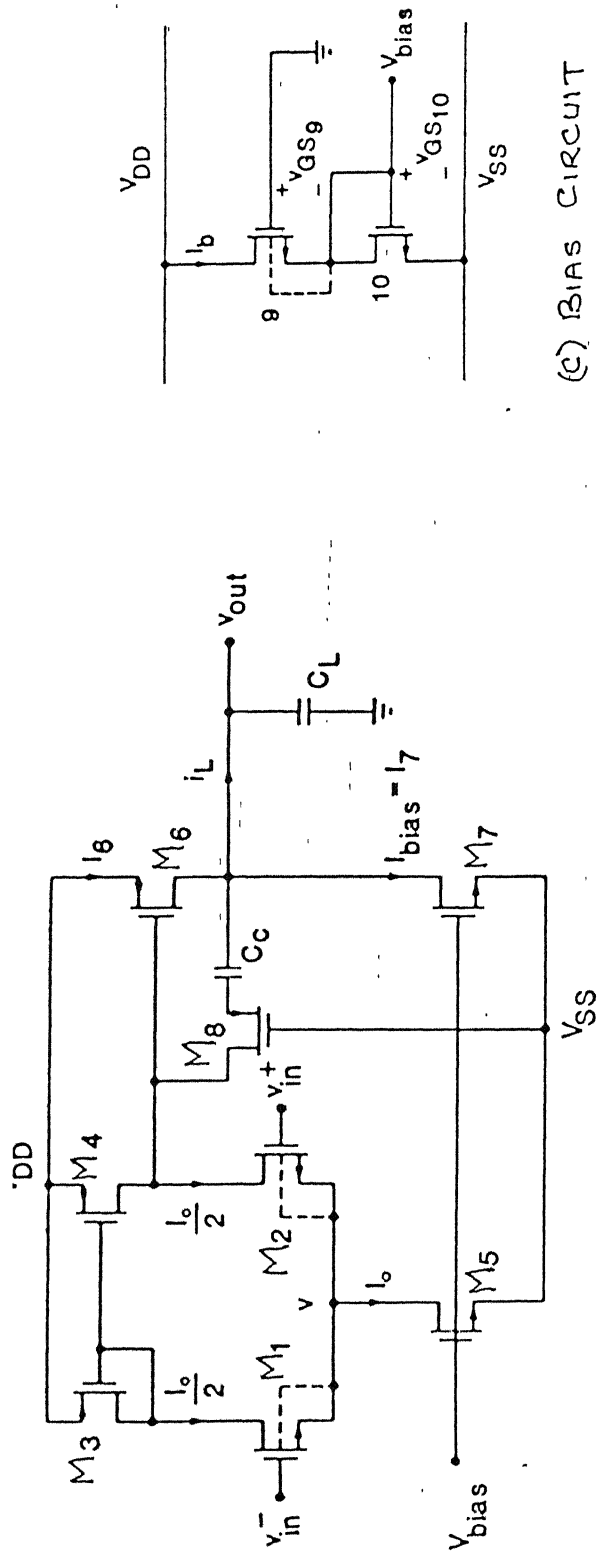
The maximum value $|i_L| = I_{bias}$ is obtained when $i_6 = 0$, i.e., when M6 is out off. Thus negative going slew rate due to output stage is,

$$S_{r0} = \frac{|i_L|}{C_L} = \frac{I_{bias}}{C_L} \quad (4.18)$$

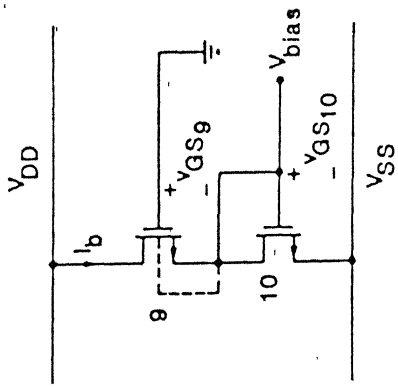
To get the frequency response consider the small signal equivalent circuit of the op-amp in figure (5.6.b). The R_O, C_O branch, as already told, is used for frequency compensation. Then the second pole of the op-amp is found to be at

$$S_{p2} = - \frac{g_{m6} C_O}{C_A (C_L + C_O) + C_L C_O} \quad (4.19)$$

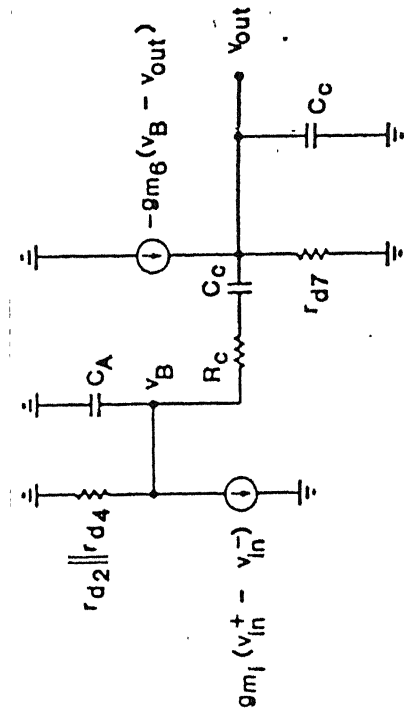
Further, if $C_A \ll C_L, C_O$ is assumed, then



(a) A TWO STAGE CMOS OP-AMP



(c) BIAS CIRCUIT



(b) SMALL SIGNAL EQUIVALENT CIRCUIT.

FIGURE 4.6.

$$S_{p2} \approx - \frac{g_{m6}}{C_L} \quad (4.20)$$

This is made as high as possible. Thus a choice

$$|S_{p2}| = \frac{g_{m6}}{C_L} = 3 \omega_0 = 3 g_{mi} / C_0 \quad (4.21)$$

is made, where ω_0 is the unity gain bandwidth of the input stage which equals g_{mi} / C_0 . Thus,

$$C_0 \approx 3 C_L g_{mi} / g_{m6} \quad (4.22)$$

$$\text{A good compromise is to choose } C_0 = C_L \quad (4.23)$$

In the op-amp circuit we assume identical geometries for M1, M2 and M3, M4. Assuming that all devices are in saturation,

$$V_{GS3} = V_{DS3} = V_{GS4} = V_{DS4} = V_{TP} + \left(\frac{I_O / 2}{k_P' (W/L)_3} \right)^{\frac{1}{2}} = V_{GS6} = V_{TP} + \left(\frac{I_6}{k_P' (W/L)_6} \right)^{\frac{1}{2}}$$

$$\text{Thus, } \frac{(W/L)_3}{(W/L)_6} = \frac{I_O / 2}{I_6} = \frac{(W/L)_4}{(W/L)_6} \quad (4.24)$$

From equation (4.15), for the time being neglecting I_6 we get,

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{I_O / 2}{I_{bias}} \quad (4.25)$$

Hence

$$g_{m6} = g_{m3} = g_{m4} = \left(\frac{(W/L)_3}{(W/L)_6} \frac{I_O}{2 I_{bias}} \right) g_{m6} = \frac{I_O / 2}{I_{bias}} \quad (4.26)$$

Then, assuming $g_d \approx \lambda i_d^0$,

$$A_O = \frac{g_{m1} g_{m6}}{(g_{d1} + g_{d1}) (g_{d6} + g_{d7})} \approx \frac{g_{m1} g_{m6}}{(\lambda I_O) (2\lambda I_{bias})} \quad (4.27)$$

$$CMRR = 2 \frac{g_{m1} g_{m1}}{g_{d6} g_{d1}} \approx \frac{2 g_{m1} g_{m1}}{(\lambda I_O) (\lambda I_O / 2)} \quad (4.28)$$

From small signal equivalent circuit the zero is at

$$S_z = - \frac{1}{(R_O - \frac{1}{g_{m6}}) C_O}$$

$$\text{giving, } R_O = \frac{1}{|S_z| C_O} + \frac{1}{g_{m6}} \quad (4.29)$$

As M8 is in the linear region

$$\frac{1}{R_O} = \left| \frac{\partial I_O}{\partial V_O} \right| = \mu C_{ox} \left(\frac{W}{L} \right)_8 |V_{GS8} - V_T| = 2 k' \left(\frac{W}{L} \right)_8 (|V_{SS} - V_{DS}| - |V_T|) \quad (4.30)$$

$$\text{also, } g_m = 2 \left(k' \left(\frac{W}{L} \right) I_O^0 \right)^{\frac{1}{2}} \quad (4.31)$$

$$\text{Hence, } \left(\frac{W}{L} \right)_1 = \left(\frac{W}{L} \right)_2 \approx \frac{g_{m1}^2}{4 k_n' (I_O / 2)} \quad (4.32)$$

$$\text{and } \left(\frac{W}{L} \right)_3 = \left(\frac{W}{L} \right)_4 \approx \frac{g_{m1}^2}{4 k_p' (I_O / 2)} \quad (4.33)$$

For filter output stages, the op-amps require to drive high capacitive loads and high currents. Hence for such applications, a class AB output stage is useful. The circuit is shown in figure (4.7). The analysis can be carried out similarly as above. In this circuit the combination of M9 and M10 act as a level shifter stage. These should be dimensioned such that the voltages V_{GS6} and V_{GS7} and hence the quiescent drain currents of M6 and M7 are not too large. Since the gates of both M6 and M7 are driven by signal voltages, the load currents can now be much larger than the bias current for either positive or negative going V_{out} . The minimum value of the output dc bias current is thus determined only by the requirement on the transconductances g_{m6} and g_{m7} needed for a good phase margin.

In this chapter we have seen how to design CMOS operational amplifiers. In the next chapter, a software package, called SFDP, is described, which can design switched capacitor filters and operational amplifiers.

CHAPTER 5

SOFTWARE ORGANIZATION AND DESIGN EXAMPLES

In this chapter, the organization of SFDP will be described. The types of data structures used and the algorithms implemented in various routines will be discussed. Finally, some designs that have been done using SFDP will be presented.

5.1 ORGANIZATION OF SFDP

SFDP, the Switched capacitor Filter Design Package, has been developed on the HP 9000 series 800 computers operating under the UNIX operating system, using standard ANSI 'C'. While developing the program, its portability has always been kept in mind and the same program, with very little modifications, can be compiled and used in a PC/AT. The program has also been run in HP series 300 workstations with minor changes.

The organization of the software can be understood from the block diagram shown in figure (5.1). As shown, SFDP can be considered to be made up of several modules and sub-modules. The different modules are linked and the data flow between them is controlled by the program manager [PM] module. The input processor module is the interface between the user and SFDP. It is basically a file parser which parses the input file. The op-amp design manager [ODM] unit controls the design of op-amps from given user specifications. The SC filter design manager [SDM] module controls the design of switched capacitor filters. The Output processor unit formats the designed data and presents to the user as an output file.

The software works as follows: When SFDP is called, the program manager (PM) gives control to the input processor. This module asks for input and output file name. Then the input file is read and the user given values are stored in appropriate data structures. If there is some error in input file, the program

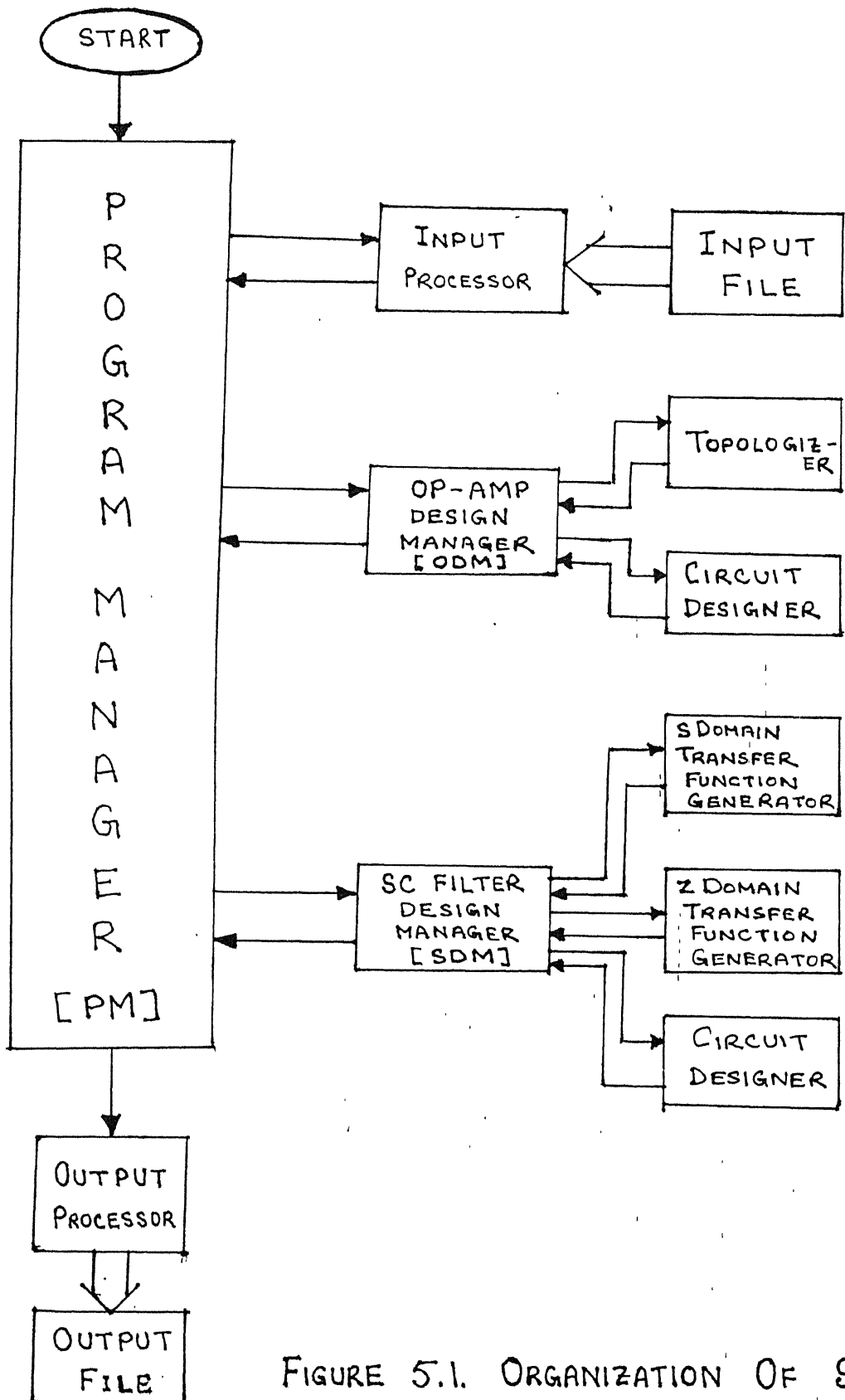


FIGURE 5.1. ORGANIZATION OF SFDP

gives an error message and terminates. When file parsing is complete, control is given back to FM.

According to the user specification, op-amp design manager (ODM) is called, if an op-amp is to be designed. ODM calls the sub-block topologizer, which chooses the appropriate circuit topology for the design. Then the circuit designer block is then called which designs the op-amp circuit using equations derived in chapter 4. After the op-amp has been designed successfully, the control is given back to ODM.

Again depending upon the user data, FM calls the SC filter design manager (SDM) module. This controls several sub-blocks as shown in 5.1. The user data is first modified by SDM. Prewarping is done to counter sampling effects. This data is then fed to the s-domain transfer function generator module. The transfer function is generated using the theories described in chapter 2. The s-domain transfer function is then converted to z-domain by the z-domain transfer function generator. This transfer function is then fed to the SC circuit designer and an SC cascade filter is obtained. These modules use the theory developed in chapter 3.

The informations that are generated are fed to the output processor. This module formats the data to make it user friendly and presents it as an output file, the name of which has been provided by the user.

At all the levels, there is a chance of error. So a rigorous error checking is made. If somewhere an error is detected, an error message is generated and the program is terminated.

5.2 DESIGN EXAMPLES

We will now present some designs done using SFDP. The software, as already mentioned, is basically to design switched capacitor filters. Also, SFDP can be used to design op-amps [25],[26], having a topology as given in chapter 4, separately. We will start this section with the design of two such op-amps. Then we will design four different types of SC filters, a low pass, a high pass, a band pass and a band reject one.

Design 1. A two stage CMOS OP-AMP

The specifications of this op-amp are as follows:

Low-Frequency gain	$A_0 \geq 70 \text{ dB}$
Unity-gain Frequency	$f_0 \geq 2 \text{ MHz}$
Slew Rate	$S_r \geq 2 \text{ V}/\mu\text{s}$
Common mode Rejection Ratio	$\text{CMRR} \geq 80 \text{ dB}$
Phase Margin	$\phi_M \geq 60^\circ$
Load Impedance	$C_L = 10 \text{ pF}$
dc supply voltages	$V_{DD} = -V_{SS} = 5 \text{ V}$

Also, it is given that the transconductance factor $k' \equiv \mu C_{ox}/2 = 30 \mu\text{A}/\text{V}^2$ for the NMOS device and $12 \mu\text{A}/\text{V}^2$ for the PMOS one. The threshold voltages are given to be $V_{TN} = 1.2 \text{ V}$ and $V_{TP} = -1.0 \text{ V}$. The channel length modulation constant $\lambda = 0.03 \text{ V}^{-1}$ and the minimum feature length is given to be 10 micron.

These values are fed to SFDP through an input file. The syntax to be used for the input file is discussed in the appendix. As the low frequency gain requirement is moderate, the two stage CMOS op-amp circuit, presented in chapter 4, figure (4.6) is suitable. The component values are determined by SFDP and given in the output file in a tabular form. A portion of SFDP output showing the circuit netlist is given in table (5.1). As seen, W and L values of all the transistors are provided along with the capacitor values. Approximate values of the important parameters are also provided.

To check the accuracy of the design, a SPICE [23] simulation of the circuit is done. The simulation results are shown in graphical form. Figure (5.2) shows the gain and phase response of the op-amp. It is seen that the unity-gain bandwidth f_0 is about 2.5 MHz and the low frequency gain A_0 is about 77 dB. Also the phase margin of the op-amp is about 90° . Thus all the specifications are met. The open loop slew rates of the op-amp are shown in figure (5.3). Figure (5.3a) is for positive input step and figure (5.3b) is for a negative input step. It is seen that for both the cases slew rate S_r is over $2.5 \text{ V}/\mu\text{s}$. Hence, this specification is also satisfied. The CMRR of the op-amp is shown in figure (5.4). It is clearly over 80 dB across the full dc to unity-gain frequency range.

OPERATIONAL AMPLIFIER DESIGN

The Designed Values are as follows :

Total number of transistors: 10
 Total number of PMOS: 4
 Total number of NMOS: 6
 Total number of capacitors: 1
 Positive Supply is connected to Node 1
 Negative Supply is connected to Node 2
 Positive input is connected to Node 5
 Negative input is connected to Node 4
 Output is from Node 8

Transistor parameters:

Number	Type	Source	Gate	Drain	Body	L	W
1	NMOS	3	4	6	3	10	66
2	NMOS	3	5	7	3	10	66
3	PMOS	1	6	6	1	10	54
4	PMOS	1	6	7	1	10	54
5	NMOS	2	9	3	2	10	54
6	PMOS	1	7	8	1	10	283
7	NMOS	2	9	8	2	10	140
8	PMOS	10	2	7	10	10	11
9	NMOS	9	0	1	9	67	10
10	NMOS	2	9	9	2	10	27

TABLE 5.1.

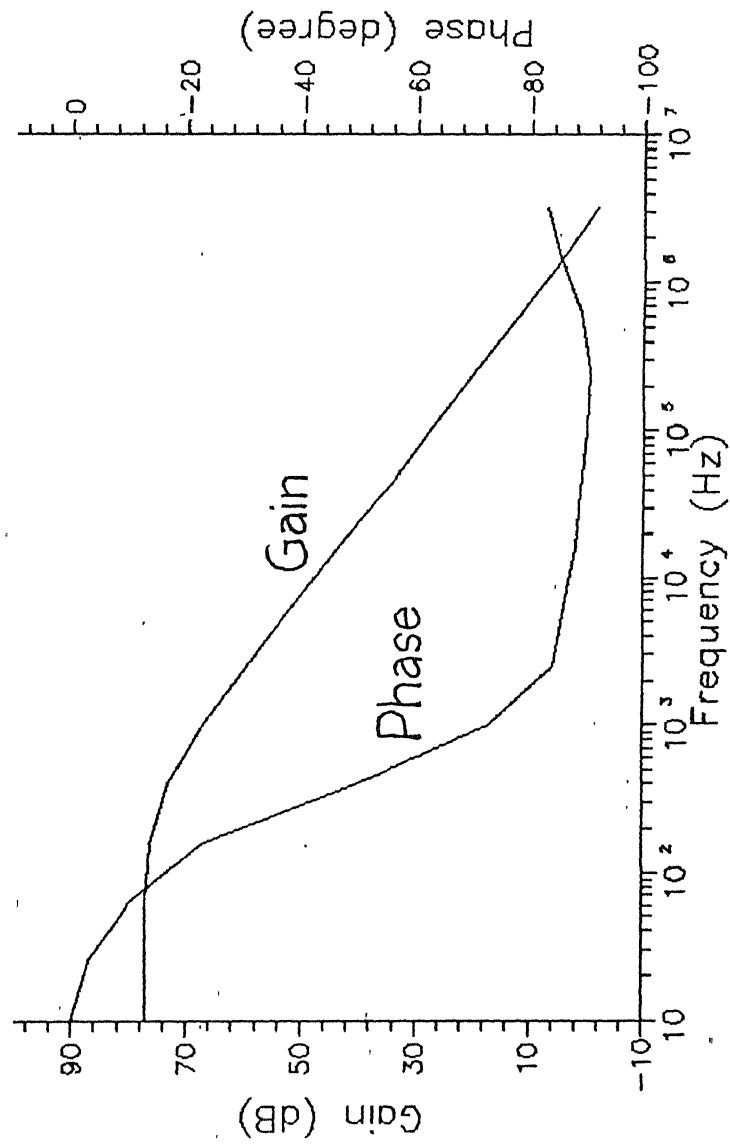


FIGURE 5.2. Gain and Phase Response

(a) Step Response of OP-AMP
for positive input step

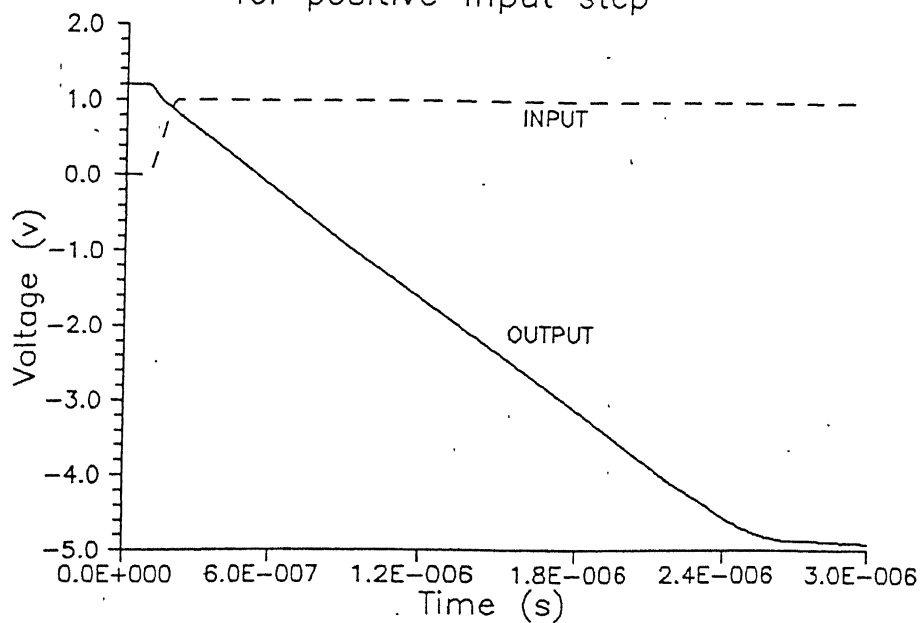
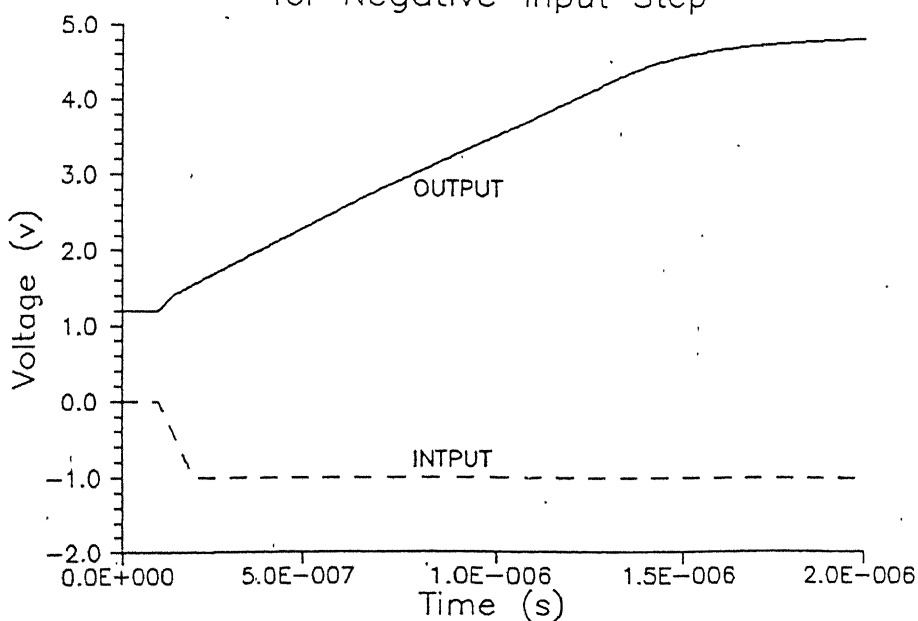


FIGURE 5.3.

(b) Step Response of OP-AMP
for Negative Input Step



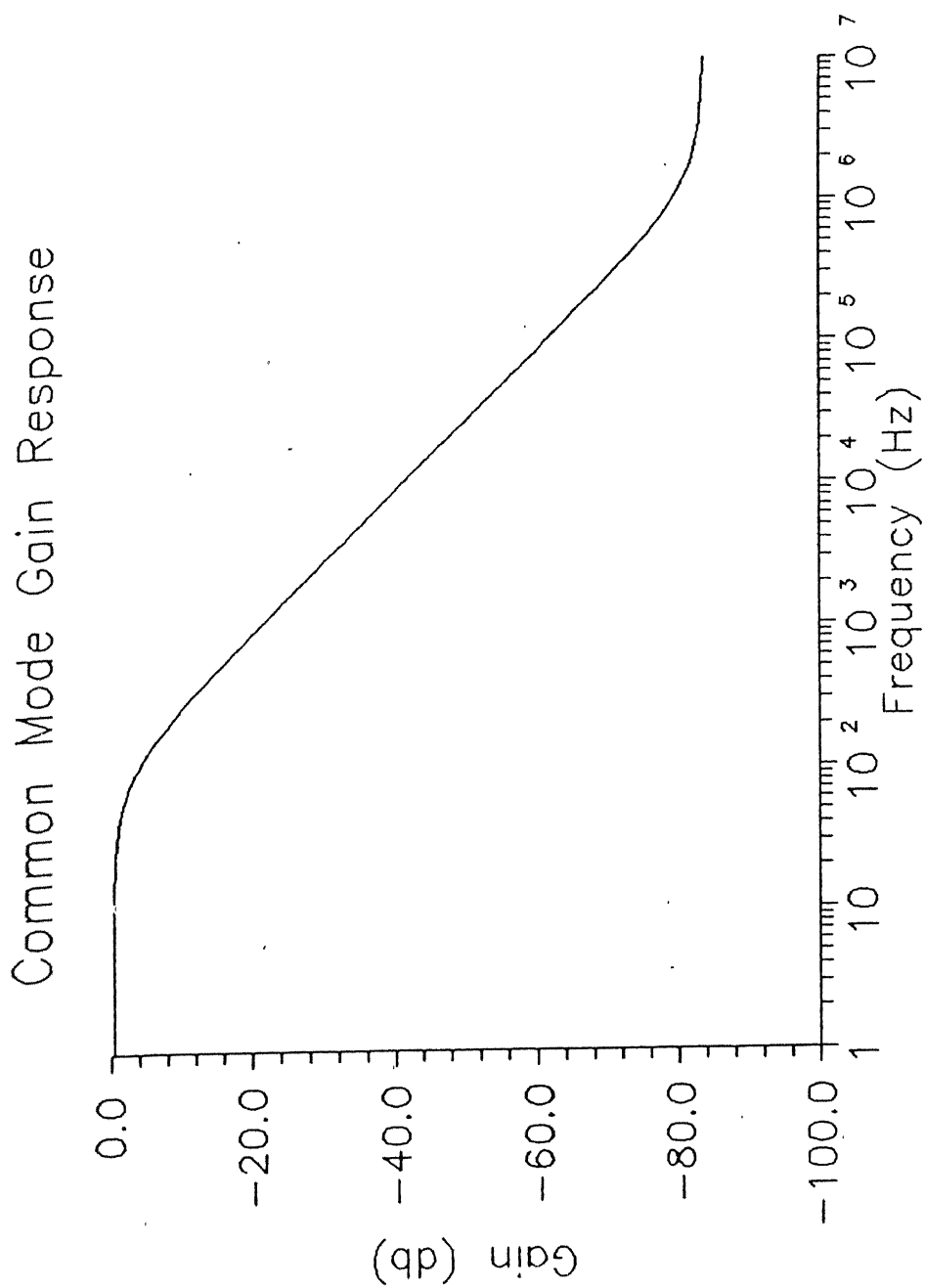


FIGURE 5.4.

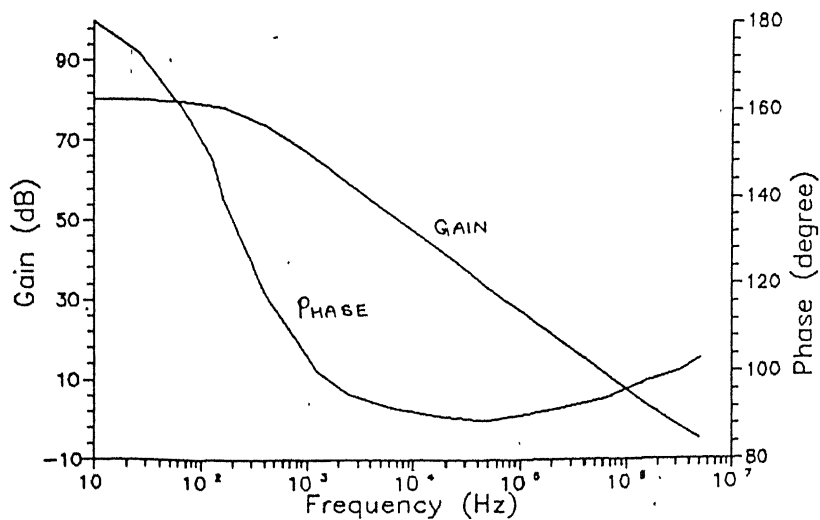


FIGURE 5.5. GAIN AND PHASE RESPONSE

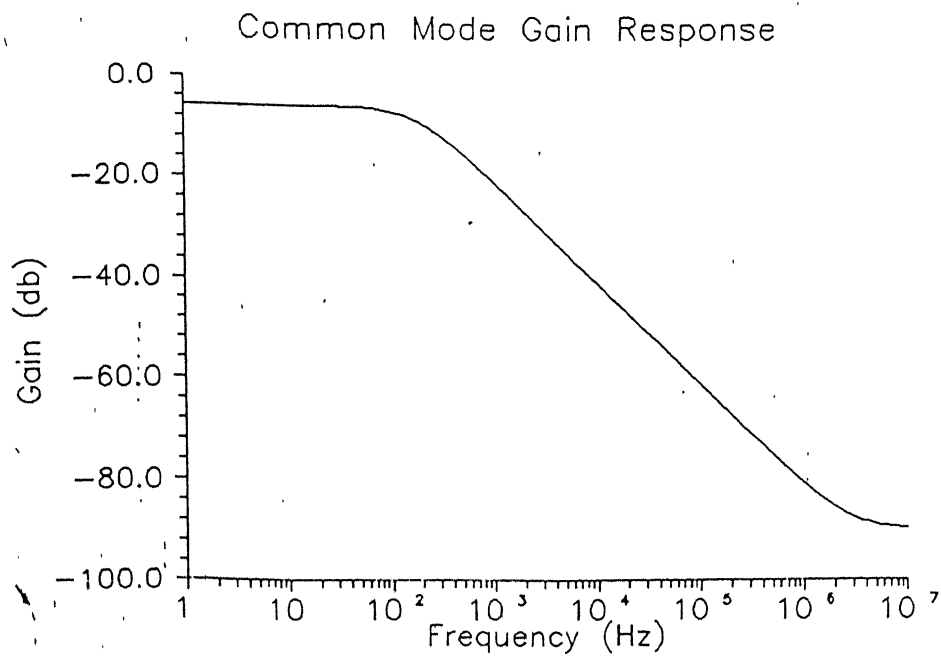


FIGURE 5.6.

The Designed Values are as follows :

Total number of transistors: 13
 Total number of PMOS: 5
 Total number of NMOS: 8
 Total number of capacitors: 1
 Positive Supply is connected to Node 1
 Negative Supply is connected to Node 2
 Positive input is connected to Node 5
 Negative input is connected to Node 4
 Output is from Node 8

Transistor parameters:

Number	Type	Source	Gate	Drain	Body	L	W
1	NMOS	3	4	6	3	10	66
2	NMOS	3	5	7	3	10	66
3	PMOS	1	6	6	1	10	54
4	PMOS	1	6	7	1	10	54
5	NMOS	2	9	3	2	10	54
6	PMOS	1	7	8	1	10	134
7	NMOS	2	11	8	2	10	67
8	PMOS	10	2	7	10	15	10
9	NMOS	11	7	1	11	177	10
10	NMOS	2	9	11	2	10	70
11	PMOS	1	12	12	1	10	54
12	NMOS	9	12	12	9	462	10
13	NMOS	2	9	9	2	10	27

The Capacitor values are:

Left Node: 10 Right Node: 8 Value: 10 picofarad

TABLE 5.2.

Numerator:

$$\begin{aligned}s^0 &= 2.08166 \times 10^{16} \\ s^1 &= 0.0 \\ s^2 &= 3.1237 \times 10^8 \\ s^3 &= 0.0 \\ s^4 &= 1.0\end{aligned}$$

Denominator:

$$\begin{aligned}s^0 &= 8.09139 \times 10^{18} \\ s^1 &= 3.3329 \times 10^{15} \\ s^2 &= 7.85602 \times 10^{11} \\ s^3 &= 1.28912 \times 10^8 \\ s^4 &= 12321.1 \\ s^5 &= 1.0\end{aligned}$$

Constant: 388.698.

This function has been plotted in figure (5.7a). As can be seen, the transfer function satisfies the frequency band requirements exactly. The stop band loss is also seen to be well over the specified value of 38.0 dB. The actual minimum loss is given by SFDP to be more than 39 dB. The pass band response of the transfer function is shown in figure (5.7b). It is seen that the maximum ripple is around 0.045 dB, which satisfies the requirements of 0.05 dB ripple.

The transfer function in the z domain is plotted in figure (5.8a). The curve is very much similar to that obtained in figure (5.7) and satisfies all the requirements. Finally, the circuit netlist given in the output file is shown in table (5.3).

Design 4. An SC High Pass Filter

Now an SC high pass filter is designed using SFDP. The specifications are similar to the previous design. Only the positions of stop band and pass band are interchanged. Thus, the specifications are:

Lower Pass Band Frequency	$f_p = 1500.0$ Hertz.
Upper Stop Band Frequency	$f_s = 1000.0$ Hertz.
Maximum Pass Band Ripple	$A_p = 0.05$ dB.
Minimum Stop Band Loss	$A_s = 38.0$ dB.

(a) LPF Transfer Function in s Domain

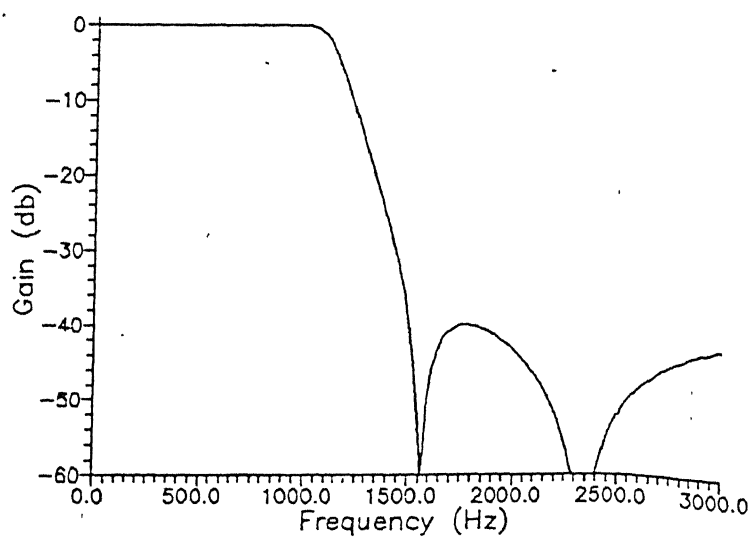
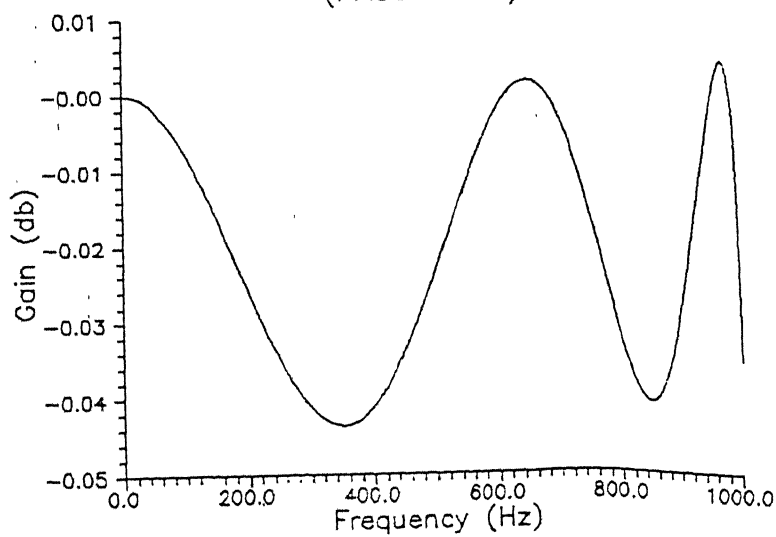


FIGURE 5.7.

(b) LPF Transfer Function in s Domain
(PASS BAND)

LPF Transfer Function in z Domain

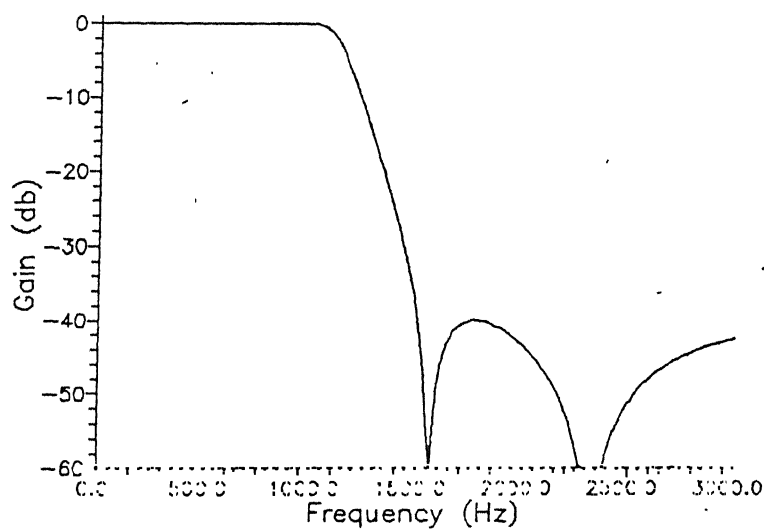


FIGURE 5.8.

HPF Transfer Function in z Domain

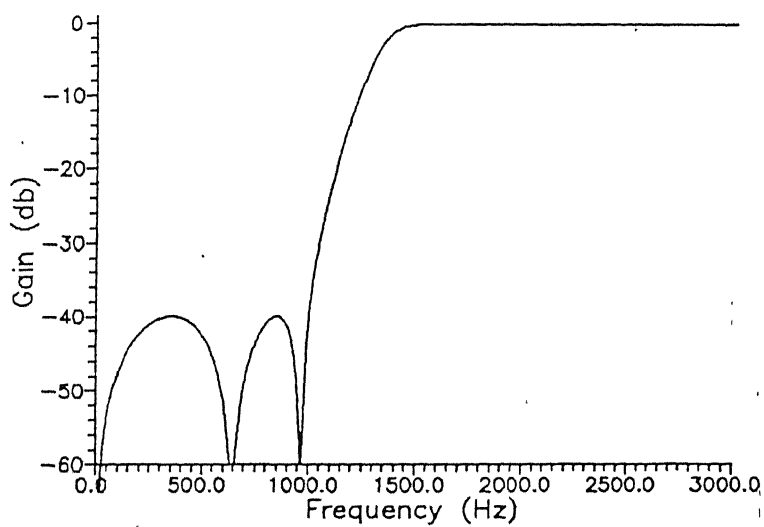


FIGURE 5.9.

SC LOW PASS FILTER DESIGN

Designed Cascade Filter Circuit:

Biquad: 1

Linear Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
1	1	1	NMOS	1	1	2	1
		2	PMOS	1	3	2	1
2	2	3	NMOS	2	2	0	2
		4	PMOS	2	4	0	2
3	1	5	NMOS	3	1	0	3
		6	PMOS	3	3	0	3
4	2	7	NMOS	3	2	4	3
		8	PMOS	3	4	4	3
5	2	9	NMOS	7	2	4	7
		10	PMOS	7	4	4	7
6	2	11	NMOS	6	2	5	6
		12	PMOS	6	4	5	6
7	1	13	NMOS	6	1	0	6
		14	PMOS	6	3	0	6

Capacitor	Left Node	Right Node	Value
1	2	3	2.000000
2	1	7	1.000000
3	3	6	2.000000
4	4	5	19.996450

OP-AMP	-ive Input	+ive Input	Output
1	4	0	5

Biquad: 2

Low Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
8	2	15	NMOS	8	2	9	8
		16	PMOS	8	4	9	8
9	1	17	NMOS	9	1	0	9
		18	PMOS	9	3	0	9
10	1	19	NMOS	10	1	0	10
		20	PMOS	10	3	0	10
11	2	21	NMOS	10	2	11	10
		22	PMOS	10	4	11	10
12	1	23	NMOS	12	1	13	12
		24	PMOS	12	3	13	12
13	2	25	NMOS	13	2	0	13
		26	PMOS	13	4	0	13
14	1	27	NMOS	14	1	0	14
		28	PMOS	14	3	0	14
15	2	29	NMOS	14	2	15	14
		30	PMOS	14	4	15	14
16	2	31	NMOS	16	2	18	16
		32	PMOS	16	4	18	16
17	2	33	NMOS	17	2	16	17
		34	PMOS	17	4	16	17
18	1	35	NMOS	17	1	0	17
		36	PMOS	17	3	0	17

Capacitor	Left Node	Right Node	Value
5	9	10	1.000000

[74]

6	11	12	11.557135
7	13	14	1.278446
8	15	16	7.910459
9	14	17	1.000000
10	10	17	1.070969
11	9	14	0.000000
12	8	15	1.308014

OP-AMP	-ive Input	+ive Input	Output
2	11	0	12
3	15	0	16

Biquad: 3

High Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
19	2	37	NMOS	19	2	20	19
		38	PMOS	19	4	20	19
20	1	39	NMOS	20	1	0	20
		40	PMOS	20	3	0	20
21	1	41	NMOS	21	1	0	21
		42	PMOS	21	3	0	21
22	2	43	NMOS	21	2	22	21
		44	PMOS	21	4	22	21
23	1	45	NMOS	23	1	24	23
		46	PMOS	23	3	24	23
24	2	47	NMOS	24	2	0	24
		48	PMOS	24	4	0	24
25	1	49	NMOS	25	1	0	25
		50	PMOS	25	3	0	25
26	2	51	NMOS	25	2	26	25
		52	PMOS	25	4	26	25
27	2	53	NMOS	27	2	29	27
		54	PMOS	27	4	29	27
28	2	55	NMOS	28	2	27	28
		56	PMOS	28	4	27	28
29	1	57	NMOS	28	1	0	28
		58	PMOS	28	3	0	28

Capacitor	Left Node	Right Node	Value
13	20	21	1.000000
14	22	23	16.429161
15	24	25	1.000000
16	26	27	7.460088
17	22	27	3.824111
18	21	28	2.308953
19	19	22	0.000000
20	19	26	1.594116

OP-AMP	-ive Input	+ive Input	Output
4	22	0	23
5	26	0	27

TABLE S.3. CONTINUED

Clock Frequency	$f_C = 50.0 \text{ K Hertz.}$
Minimum Capacitance	$C_{\min} = 1.0 \text{ pF.}$

Again FSDP designs a fifth order filter. The s domain transfer function along with the z domain transfer function is shown in table (5.4). The z domain transfer function is plotted in figure (5.9). From the figure we see that all the specifications are satisfied. The circuit netlist is given in table (5.4).

Design 5. An SC Band Pass Filter

The filter specifications are given as,

Lower Pass Band Frequency	$f_{p1} = 1900.0 \text{ Hertz.}$
Upper Pass Band Frequency	$f_{p2} = 2100.0 \text{ Hertz.}$
Lower Stop Band Frequency	$f_{s1} = 1700.0 \text{ Hertz.}$
Upper Stop Band Frequency	$f_{s2} = 2300.0 \text{ Hertz.}$
Maximum Pass Band Ripple	$A_p = 0.1 \text{ dB}$
Minimum Stop Band Loss	$A_s = 30.0 \text{ dB.}$
Clock Frequency	$f_C = 50.0 \text{ K Hertz.}$
Minimum Capacitance	$C_{\min} = 1.0 \text{ pF.}$

SFDP designs a band pass filter of sixth order. The z domain filter is plotted in figure (5.10). It can be seen that all the specifications are satisfied. The designed circuit netlist is given in table (5.5) .

Design 6. An SC Band Reject Filter

Finally, a band reject filter is designed. The specifications are similar to design 5. These are

Lower Pass Band Frequency	$f_{p1} = 1700.0 \text{ Hertz.}$
Upper Pass Band Frequency	$f_{p2} = 2300.0 \text{ Hertz.}$
Lower Stop Band Frequency	$f_{s1} = 1900.0 \text{ Hertz.}$
Upper Stop Band Frequency	$f_{s2} = 2100.0 \text{ Hertz.}$
Maximum Pass Band Ripple	$A_p = 0.1 \text{ dB.}$
Minimum Stop Band Loss	$A_s = 30.0 \text{ dB.}$
Clock Frequency	$f_C = 50.0 \text{ K Hertz.}$
Minimum Capacitance	$C_{\min} = 1.0 \text{ pF.}$

SC HIGH PASS FILTER DESIGN

Switched Capacitor Filter Design

Filter Type HIGH PASS FILTER
ORDER of the designed filter: 5

Transfer function in the s domain:

Numerator:

$s^0 = 0$
 $s^1 = 7.98434e+15$
 $s^2 = 0$
 $s^3 = 7.05155e+08$
 $s^4 = 0$
 $s^5 = 13.2863$

Denominator:

$s^0 = 7.54742e+19$
 $s^1 = 1.56364e+16$
 $s^2 = 2.75086e+12$
 $s^3 = 2.81881e+08$
 $s^4 = 20108.3$
 $s^5 = 0.820849$

Constant: 0.0617817

Transfer function in the z domain:

Numerator

$z^0 = -1.00000$
 $z^1 = 4.97583$
 $z^2 = -9.93660$
 $z^3 = 9.93660$
 $z^4 = -4.97583$
 $z^5 = 1.00000$

Denominator

$z^0 = -0.61285$
 $z^1 = 3.35365$
 $z^2 = -7.36508$
 $z^3 = 8.11860$
 $z^4 = -4.49408$
 $z^5 = 1.00000$

Constant: 0.78365

Transfer function of the BIQUADS:

Biquad number: 1

Linear Section

Numerator: -1.00000 1.00000
 Denominator: -0.77798 1.00000

Biquad number: 2

Low Q Section

Numerator: 1.00000 -1.99022 1.00000
 Denominator: 0.81917 -1.78311 1.00000
 Quality Factor = 0.996433

Biquad number: 3

High Q Section

Numerator: 1.00000 -2.00000 1.00000
 Denominator: 0.96164 -1.93299 1.00000
 Quality Factor = 4.354127

Designed Cascade Filter Circuit:

Biquad: 1

Linear Section

[++a]

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
1	1	1	NMOS	1	1	2	1
		2	PMOS	1	3	2	1
2	2	3	NMOS	2	2	0	2
		4	PMOS	2	4	0	2
3	1	5	NMOS	3	1	0	3
		6	PMOS	3	3	0	3
4	2	7	NMOS	3	2	4	3
		8	PMOS	3	4	4	3
5	2	9	NMOS	7	2	4	7
		10	PMOS	7	4	4	7
6	2	11	NMOS	6	2	5	6
		12	PMOS	6	4	5	6
7	1	13	NMOS	6	1	0	6
		14	PMOS	6	3	0	6
Capacitor	Left Node		Right Node		Value		
1	2		3		2.000000		
2	1		7		1.000000		
3	3		6		2.000000		
4	4		5		7.008340		
OP-AMP	-ive Input		+ive Input		Output		
1	4		0		5		

Biquad: 2

Low Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
8	2	15	NMOS	8	2	9	8
		16	PMOS	8	4	9	8
9	1	17	NMOS	9	1	0	9
		18	PMOS	9	3	0	9
10	1	19	NMOS	10	1	0	10
		20	PMOS	10	3	0	10
11	2	21	NMOS	10	2	11	10
		22	PMOS	10	4	11	10
12	1	23	NMOS	12	1	13	12
		24	PMOS	12	3	13	12
13	2	25	NMOS	13	2	0	13
		26	PMOS	13	4	0	13
14	1	27	NMOS	14	1	0	14
		28	PMOS	14	3	0	14
15	2	29	NMOS	14	2	15	14
		30	PMOS	14	4	15	14
16	2	31	NMOS	16	2	16	16
		32	PMOS	16	4	16	16
17	2	33	NMOS	17	2	16	17
		34	PMOS	17	4	16	17
18	1	35	NMOS	17	1	0	17
		36	PMOS	17	3	0	17
Capacitor	Left Node		Right Node		Value		
5	9		10		1.000000		
6	11		12		16.241505		
7	13		14		1.000000		
8	15		16		5.946334		
9	14		17		1.312675		
10	10		17		4.250526		

TABLE 5.4. CONTINUED

[77b]

11	9	14	0.000000
12	8	15	6.294472

OP-AMP	-ive Input	+ive Input	Output
2	11	0	12
3	15	0	10

Biquad: 3

High Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
19	2	37	NMOS	19	2	20	19
		38	PMOS	19	4	20	19
20	1	39	NMOS	20	1	0	20
		40	PMOS	20	3	0	20
21	1	41	NMOS	21	1	0	21
		42	PMOS	21	3	0	21
22	2	43	NMOS	21	2	22	21
		44	PMOS	21	4	22	21
23	1	45	NMOS	23	1	24	23
		46	PMOS	23	3	24	23
24	2	47	NMOS	24	2	0	24
		48	PMOS	24	4	0	24
25	1	49	NMOS	25	1	0	25
		50	PMOS	25	3	0	25
26	2	51	NMOS	25	2	26	25
		52	PMOS	25	4	26	25
27	2	53	NMOS	27	2	29	27
		54	PMOS	27	4	29	27
28	2	55	NMOS	28	2	27	28
		56	PMOS	28	4	27	28
29	1	57	NMOS	28	1	0	28
		58	PMOS	28	3	0	28

Capacitor	Left Node	Right Node	Value
13	20	21	0.000000
14	22	23	6.072274
15	24	25	1.000000
16	26	27	5.747345
17	22	27	1.338786
18	21	28	1.000000
19	19	22	0.000000
20	19	26	1.276701

OP-AMP	-ive Input	+ive Input	Output
4	22	0	23
5	26	0	27

TABLE 5.4. CONTINUED

BPF Transfer Function in z Domain

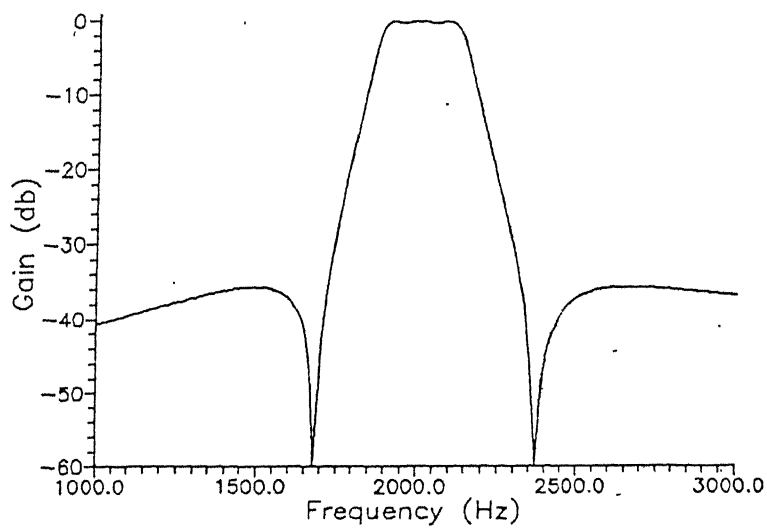


FIGURE 5.10

BRF Transfer Function in z Domain

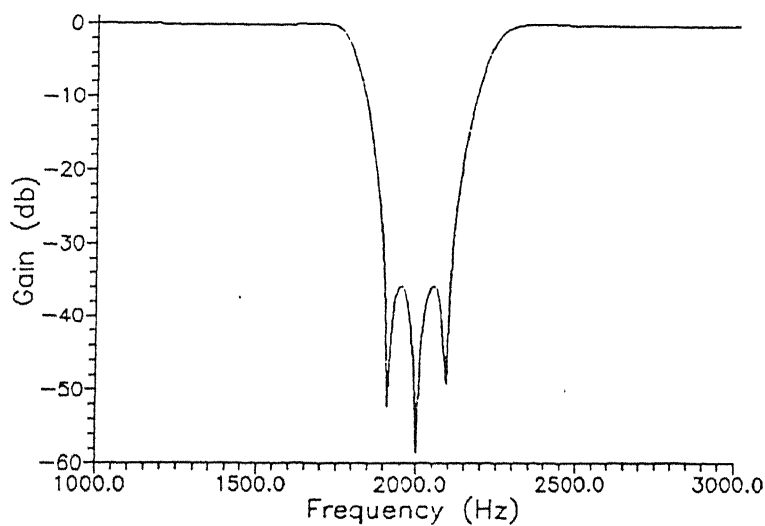


FIGURE 5.11

SC BAND PASS FILTER DESIGN

Switched Capacitor Filter Design.

Filter Type: BAND PASS FILTER
ORDER of the designed filter: 6

Transfer function in the s domain:

Numerator:

$s^0 = 0$
 $s^1 = 2.53435e+16$
 $s^2 = 0$
 $s^3 = 3.37676e+08$
 $s^4 = 0$
 $s^5 = 1$

Denominator:

$s^0 = 4.03459e+24$
 $s^1 = 6.1763e+19$
 $s^2 = 7.6696e+16$
 $s^3 = 7.79495e+11$
 $s^4 = 4.81782e+08$
 $s^5 = 2437.03$
 $s^6 = 1$

Constant = 154.564

Transfer function in the z domain:

Numerator

$z^0 = -1.00000$
 $z^1 = 3.26741$
 $z^2 = -4.73875$
 $z^3 = 0.90000$
 $z^4 = 4.73875$
 $z^5 = -3.26741$
 $z^6 = 1.00000$

Denominator

$z^0 = 0.95316$
 $z^1 = -5.58357$
 $z^2 = 13.80830$
 $z^3 = -18.44351$
 $z^4 = 14.03090$
 $z^5 = -5.76504$
 $z^6 = 1.00000$

Constant = 0.00177773

Transfer function of the BIQUADS:

Biquad number: 1 High Q Section

Numerator: -1.00000 0.00000 1.00000
Denominator: 0.97452 -1.91264 1.00000
Quality Factor = 9.625569

Biquad number: 2 High Q Section

Numerator: 1.00000 -1.93732 1.00000
Denominator: 0.98833 -1.91802 1.00000
Quality Factor = 22.448396

Biquad number: 3 High Q Section

Numerator: 1.00000 -2.00000 1.00000
Denominator: 0.98363 -1.93437 1.00000
Quality Factor = 22.448801

Designed Cascade Filter Circuit:

Biquad 1				High Q Section			
Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
1	2	1	NMOS	1	2	2	1
		2	PMOS	1	4	2	1
2	1	3	NMOS	2	1	0	2
		4	PMOS	2	3	0	2
3	1	5	NMOS	3	1	0	3
		6	PMOS	3	3	0	3
4	2	7	NMOS	3	2	4	3
		8	PMOS	3	4	4	3
5	1	9	NMOS	5	1	6	5
		10	PMOS	5	3	6	5
6	2	11	NMOS	6	2	0	6
		12	PMOS	6	4	0	6
7	1	13	NMOS	7	1	0	7
		14	PMOS	7	3	0	7
8	2	15	NMOS	7	2	8	7
		16	PMOS	7	4	8	7
9	2	17	NMOS	7	2	11	7
		18	PMOS	7	4	11	7
10	2	19	NMOS	10	2	7	10
		20	PMOS	10	4	7	10
11	1	21	NMOS	10	1	0	10
		22	PMOS	10	3	0	10
Capacitor	Left Node		Right Node	Value			
1	2	4	3	0.000000			
2	4	6	5	9.714592			
3	6	8	7	19.429184			
4	8	10	9	78.503202			
5	10	12	9	1.000000			
6	12	14	10	2.428972			
7	14	16	4	7.835012			
8	16	18	8	1.000000			
OP-AMP	-ive Input		+ive Input	Output			
1	4	6	0	5			
2	8	10	0	9			

Biquad 2				High Q Section			
Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
12	2	23	NMOS	12	2	13	12
		24	PMOS	12	4	13	12
13	1	25	NMOS	13	1	0	13
		26	PMOS	13	3	0	13
14	1	27	NMOS	14	1	0	14
		28	PMOS	14	3	0	14
15	2	29	NMOS	14	2	15	14
		30	PMOS	14	4	15	14
16	1	31	NMOS	16	1	17	16
		32	PMOS	16	3	17	16
17	2	33	NMOS	17	2	0	17
		34	PMOS	17	4	0	17
18	1	35	NMOS	18	1	0	18
		36	PMOS	18	3	0	18

TABLE 5.5. CONTINUED

19	2	37	NMOS	18	2	19	18
		38	PMOS	18	4	19	18
20	2	39	NMOS	20	2	22	20
		40	PMOS	20	4	22	20
21	2	41	NMOS	21	2	20	21
		42	PMOS	21	4	20	21
22	1	43	NMOS	21	1	0	21
		44	PMOS	21	3	0	21

Capacitor	Left Node	Right Node	Value
9	13	14	1.931275
10	15	16	22.926096
11	17	18	1.000000
12	19	20	3.736790
13	15	20	1.000000
14	14	21	6.023252
15	12	15	0.000000
16	12	19	1.343941

OP-AMP	-ive Input	+ive Input	Output
3	15	0	16
4	19	0	20

Biquad: 3

High Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
23	2	45	NMOS	23	2	24	23
		46	PMOS	23	4	24	23
24	1	47	NMOS	24	1	0	24
		48	PMOS	24	3	0	24
25	1	49	NMOS	25	1	0	25
		50	PMOS	25	3	0	25
26	2	51	NMOS	25	2	26	25
		52	PMOS	25	4	26	25
27	1	53	NMOS	27	1	28	27
		54	PMOS	27	3	28	27
28	2	55	NMOS	28	2	0	28
		56	PMOS	28	4	0	28
29	1	57	NMOS	29	1	0	29
		58	PMOS	29	3	0	29
30	2	59	NMOS	29	2	30	29
		60	PMOS	29	4	30	29
31	2	61	NMOS	31	2	33	31
		62	PMOS	31	4	33	31
32	2	63	NMOS	32	2	31	32
		64	PMOS	32	4	31	32
33	1	65	NMOS	32	1	0	32
		66	PMOS	32	3	0	32

Capacitor	Left Node	Right Node	Value
17	24	25	0.000000
18	26	27	22.740185
19	28	29	5.398212
20	30	31	22.889246
21	26	31	1.000000
22	25	32	5.327719
23	23	26	0.000000
24	23	30	1.000000

OP-AMP	-ive Input	+ive Input	Output
5	26	0	27
6	30	0	31

 SC BAND REJECT FILTER DESIGN

 Switched Capacitor Filter Design.

Filter Type: BAND REJECT FILTER
 ORDER of the designed filter: 6

Transfer function in the s domain:

Numerator:

s^0 = 4.77311e+25
 s^1 = 0
 s^2 = 9.01812e+17
 s^3 = 0
 s^4 = 5.66478e+09
 s^5 = 0
 s^6 = 11.8305

Denominator:

s^0 = 6.90387e+24
 s^1 = 2.49717e+20
 s^2 = 1.3456e+17
 s^3 = 3.19342e+12
 s^4 = 8.45245e+08
 s^5 = 9853.29
 s^6 = 1.71117

Constant = 0.144641

Transfer function in the z domain:

Numerator

z^0 = 1.00000
 z^1 = -5.81149
 z^2 = 14.25778
 z^3 = -18.89234
 z^4 = 14.25778
 z^5 = -5.81149
 z^6 = 1.00000

Denominator

z^0 = 0.89283
 z^1 = -5.28719
 z^2 = 13.21814
 z^3 = -17.84842
 z^4 = 13.72710
 z^5 = -5.70222
 z^6 = 1.00000

Constant = 0.945028

Transfer function of the BIQUADS:

Biquad number: 1

High Q Section

Numerator: 1.00000 -1.93164 1.00000
 Denominator: 0.92916 -1.86869 1.00000
 Quality Factor = 3.381942

Biquad number: 2

High Q Section

Numerator: 1.00000 -1.93732 1.00000
 Denominator: 0.97818 -1.90116 1.00000
 Quality Factor = 12.522468

Biquad number: 3

High Q Section

Numerator: 1.00000 -1.94254 1.00000
 Denominator: 0.98234 -1.93236 1.00000
 Quality Factor = 12.522468

Designed Cascade Filter Circuit:

Biquad: 1

High Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
1	2	1	NMOS	1	2	2	1
		2	PMOS	1	4	2	1
2	1	3	NMOS	2	1	0	2
		4	PMOS	2	3	0	2
3	1	5	NMOS	3	1	0	3
		6	PMOS	3	3	0	3
4	2	7	NMOS	3	2	4	3
		8	PMOS	3	4	4	3
5	1	9	NMOS	5	1	6	5
		10	PMOS	5	3	6	5
6	2	11	NMOS	6	2	0	6
		12	PMOS	6	4	0	6
7	1	13	NMOS	7	1	0	7
		14	PMOS	7	3	0	7
8	2	15	NMOS	7	2	8	7
		16	PMOS	7	4	8	7
9	2	17	NMOS	9	2	11	9
		18	PMOS	9	4	11	9
10	2	19	NMOS	10	2	9	10
		20	PMOS	10	4	9	10
11	1	21	NMOS	10	1	0	10
		22	PMOS	10	3	0	10

Capacitor	Left Node	Right Node	Value
1	2	3	1.000000
2	4	5	3.877233
3	6	7	1.000000
4	8	9	4.307062
5	4	9	1.183072
6	3	10	1.009658
7	1	4	0.000000
8	1	8	3.772684

OP-AMP	-ive Input	+ive Input	Output
1	4	0	5
2	8	0	9

Biquad: 2

High Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
12	2	23	NMOS	12	2	13	12
		24	PMOS	12	4	13	12
13	1	25	NMOS	13	1	0	13
		26	PMOS	13	3	0	13
14	1	27	NMOS	14	1	0	14
		28	PMOS	14	3	0	14
15	2	29	NMOS	14	2	15	14
		30	PMOS	14	4	15	14
16	1	31	NMOS	16	1	17	16
		32	PMOS	16	3	17	16
17	2	33	NMOS	17	2	0	17
		34	PMOS	17	4	0	17
18	1	35	NMOS	18	1	0	18

TABLE 5.6. CONTINUED

[826]

		36	PMOS	18	3	0	18
19	2	37	NMOS	18	2	19	18
		38	PMOS	18	4	19	18
20	2	39	NMOS	20	2	22	20
		40	PMOS	20	4	22	20
21	2	41	NMOS	21	2	20	21
		42	PMOS	21	4	20	21
22	1	43	NMOS	21	1	0	21
		44	PMOS	21	3	0	21

Capacitor	Left Node	Right Node	Value
9	13	14	1.072189
10	15	16	12.930252
11	17	18	1.000000
12	19	20	3.543677
13	15	20	1.000000
14	14	21	3.528751
15	12	15	0.000000
16	12	19	1.322911

OP-AMP	-ive Input	+ive Input	Output
3	15	0	16
4	19	0	20

Biquad: 3

High Q Section

Switch	Phase	Transistor	Type	Source	Gate	Drain	Body
23	2	45	NMOS	23	2	24	23
		46	PMOS	23	4	24	23
24	1	47	NMOS	24	1	0	24
		48	PMOS	24	3	0	24
25	1	49	NMOS	25	1	0	25
		50	PMOS	25	3	0	25
26	2	51	NMOS	25	2	26	25
		52	PMOS	25	4	26	25
27	1	53	NMOS	27	1	28	27
		54	PMOS	27	3	28	27
28	2	55	NMOS	28	2	0	28
		56	PMOS	28	4	0	28
29	1	57	NMOS	29	1	0	29
		58	PMOS	29	3	0	29
30	2	59	NMOS	29	2	30	29
		60	PMOS	29	4	30	29
31	2	61	NMOS	31	2	33	31
		62	PMOS	31	4	33	31
32	2	63	NMOS	32	2	31	32
		64	PMOS	32	4	31	32
33	1	65	NMOS	32	1	0	32
		66	PMOS	32	3	0	32

Capacitor	Left Node	Right Node	Value
17	24	25	1.558600
18	26	27	12.471733
19	28	29	1.000000
20	30	31	4.540066
21	26	31	1.000000
22	25	32	2.829777
23	23	26	0.000000
24	23	30	2.174802

OP-AMP	-ive Input	+ive Input	Output
5	26	0	27
6	30	0	31

TABLE 5.6. CONTINUED

The designed filter is again of order six. The z domain plot is shown in figure (5.11). All the specifications are met. A netlist of the designed circuit is given in table (5.6).

From the above designs we see that in all the cases, the specifications have been satisfied. The s domain transfer function obtained in design 3 has been compared with the transfer function given in reference 4, page 102. The coefficients match upto third decimal place. This shows the accuracy of the s domain elliptic filter transfer function generator of SFDP. The designed circuit of example 3 has also been compared with the results given in reference 14. Here also the component values are seen to be in excellent agreement. The design of example 5 has been compared with that in reference 10. Again an equivalent design has been obtained. Due to the unavailability of a switched capacitor circuit simulator [24], the designed circuits were not simulated. But from the above discussions one can see that the circuits designed by SFDP are quite accurate.

CHAPTER 6

CONCLUSIONS

6.1 SUMMARY OF THE WORK DONE

In this work, a software package for the design of switched capacitor cascade filters, called SFDP, has been developed. The package designs cascade filter circuits from given frequency domain specifications. A sub module for the design of operational amplifier, an essential building block for SC filter circuits, has also been included in SFDP. The specifications can be given to SFDP through an input file and the designed circuit netlist along with the filter transfer functions are provided in an output file.

While developing SFDP, portability of the software has been kept in mind. The software has been developed using the HP 9000 series of computers running the UNIX operating system. It can also be used on a PC/AT with only minor modifications. Extensive error checking has been included in the software to make it user friendly. An error message is generated whenever necessary.

Several designs have been performed using SFDP. In all the cases the user requirements have been satisfied. The operational amplifier circuits designed by SFDP has been simulated using SPICE. The results, like dc gain, unity-gain bandwidth, phase margin, CMRR etc., are in excellent agreement with the specifications.

The filter transfer functions that are synthesized by SFDP are also quite accurate. Some of the transfer function plots have been given in chapter 5. It can be clearly seen from those curves that the specifications are satisfied. The transfer functions obtained from SFDP have also been compared with those given in reference [11]. It is seen that the transfer function coefficients match upto third decimal place. Some of the designed circuits have been compared with those given in references [10] and [14]. They are also in excellent agreement.

6.2 SUGGESTIONS FOR FUTURE WORK

Some of the areas in which future work can concentrate are now discussed.

(1) **SFDP** presently can design SC filters using coupled biquad structures only. One extension will be to include design of ladder filters and N-path filters. For designing such filters, the elliptic filter transfer function generator routine of **SFDP** can be used. Other modules will have to be written separately.

(2) Another possible improvement is to include an analysis program for switched capacitor circuits, similar to the **SWITCAP** [24] program. This will enhance the accuracy of the design and much more flexible designs will be possible. Simulation of the circuits will then be possible, which can be used by **SFDP** for fine tuning of the design. Also, **SPICE** can be used in an interactive way with **SFDP** for analysis; this will be useful particularly for the operational amplifier design.

(3) The **SFDP** program has been developed for standard monochrome displays and so interactive graphics facilities have not been included. Using a workstation these facilities can be provided. Such facilities may use an editor to manually place the poles and zeros in the s or z plane and a window displaying the transfer function curves for user feedback. If a workstation is used, **SFDP** can be modified to make it a menu driven program, making it more user friendly and interactive. But, if these facilities are included, the portability of the program will be lost.

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APPENDIX

SFDP USER MANUAL

This appendix is a user manual for the software package SFDP. The package is for the design of switched capacitor cascade filters. It can be also programmed for the design of CMOS op-amps of topologies as given in chapter 4 of this thesis. The op-amps are mainly for use in the SC filters. In this appendix we will give the syntax that has to be followed to write an input file for SFDP.

A. INPUT FORMAT

The input format of SFDP is of the free format type. The input parser is not case sensitive, i.e., upper and lower case characters can be mixed. The input file for SFDP should have the following main blocks.

In the value field, one can give an integer or a floating point number whichever is suitable. The actual units are as given in the above tables and are not to be given in the input file. However, a scaling factor may be given with the value. the following scaling factors are permissible:

G = 1.0E9 MEG = 1.0E6 K = 1.0E3 M = 1.0E-3
U = 1.0E-6 N = 1.0E-9 P = 1.0E-12

Lower case characters may be used.

A.1. Title Card.

This should be the first line in the input file. The total number of characters can be at the maximum 80. This title is used by SFDP to mark the start of a new section in the output file.

Example:

SC FILTER DESIGN

A.2. Comments

Comments can be written between two sub blocks in the input file. It should start and end with *.

Example:

```
* Filter Input Specifications *
```

A.3. Sub-Blocks

The sub-blocks are for specifying different parameters and specifications. Each sub-block consists of a block header and a list of parameters. The syntax for such sub-blocks is of the form:

```
#(Header name) [
    ... List of parameters ...
]
```

The header name should be preceded by a #. This symbol marks the beginning of a block. As seen, the parameter list can be written in several lines. Only restriction being that these should be inside third braces as shown. In the parameter list, each parameter has a name and optionally a value. There should be one (or more) gap(s) between a name and the corresponding value. Each such couple should be separated by a comma. Thus a block has a form,

```
#(Header name) [
    (name1) (value1), (name2) (value2),
    (name3) (value3)
]
```

The following is a list of possible header names:

```
PPM    → The Process Parameters.
OPM    → Operational Amplifier Specifications.
FILTER → Filter Specifications.
PLOT   → Plotting Informations
PRINT  → Printing Informations.
```

A.3.1. PROCESS PARAMETERS

The process parameters are to be given as follows

```
#PPM [ KP (value), KN (value), VTN (value), VTP (value),
      LAMBDA (value), VDD (value), VSS (value), MFS (value), CMIN (value) ]
```

Description

Name	Parameter	Unit	Default
KP	PMOS transconductance factor ($\mu C_{ox}/2$)	A/V ²	10.0 μ A/V ²
KN	NMOS transconductance factor ($\mu C_{ox}/2$)	A/V ²	30.0 μ A/V ²
VTN	NMOS threshold voltage (V_{Tn})	V	1.0V
VTP	PMOS threshold voltage (V_{Tp})	V	-1.0V
LAMBDA	Channel length modulation (λ)	V ⁻¹	0.03V ⁻¹
VDD	Positive Supply (V_{DD})	V	5.0V
VSS	Negative Supply (V_{SS})	V	-5.0V
MFS	Minimum feature size	m	10.0 μ m
CMIN	Minimum capacitance realizable	F	1.0pF

A.3.2. Operational Amplifier Specifications

The specifications are given as follows:
#OP_AMP [AD (value), FO (value), SR (value), CMRR (value),
 PHM (value), LOAD (value), <OPTSTG>]

Description:

Name	Parameter	Unit	Default
AD	Low Frequency Gain (A_D)	dB	50dB
FO	Unity-gain Frequency	Hz	1.0MHz
SR	Slew Rate (S_R)	V/ μ s	1.0M
CMRR	Common Mode Rejection Ratio	dB	50.0dB
PHM	Phase Margin (ϕ_M)	degree	60°
LOAD	Capacitive Load	F	1.0pF

OPTSTG → Output stage. When this is used, SFDP uses a push-pull output stage.

A.3.3. Filter Specifications

The specifications are given as follows:

#FILTER [TYPE (value), AS (value), AP (value), FC (value),
 FP (value), FS (value), FP1 (value), FP2 (value),
 FS1 (value), FS2 (value)]

Description.

TYPE is the type of filter to be designed. Thus it can have one of the four

LPF → Low Pass Filter
 HPF → High Pass Filter
 BPF → Band Pass Filter
 BRF → Band Reject Filter

Name	Parameter	Unit	Default
AS	Minimum Stop Band Loss	dB	10.0dB
AP	Maximum Pass Band Loss	dB	1.0dB
FC	Clock Frequency	Hz	10.0kHz
FP	Pass Band Corner Frequency (for LPF and HPF case only)	Hz	0.0
FS	Stop Band Corner Frequency (for LPF and HPF case only)	Hz	0.0
FP1,	Lower and Upper Pass Band Frequency	Hz	0.0
FP2	(for BPF and BRF case only)		
FS1,	Lower and Upper Stop Band Frequency	Hz	0.0
FS2	(for BPF and BRF case only)		

A.3.4. PLOT

This sub-block is for specifying which transfer function to plot and how to plot it. It is to be specified as follows:

```
#PLOT [
    <LPPTRF> <LHL> <RHL> <points>
    <SDNTRF> <LHL> <RHL> <points>
    <SDTRF>   <LHL> <RHL> <points>
    <ZDTRF>   <LHL> <RHL> <points>
```

]

Description:

LPPTRF → Low Pass Prototype Transfer Function.
 SDNTRF → Normalized s Domain Transfer Function.
 SDTRF → Denormalized s Domain Transfer Function.
 ZDTRF → z Domain Transfer Function.
 LHL → Starting Frequency to Plot.
 RHL → End Frequency upto which to Plot.
 points → Number of Points to Plot.

A.3.5. PRINT

This is used for printing different transfer functions. It is exactly similar to PLOT sub-block. Only header name #PRINT instead of PLOT.

In all the cases, if some parameter values are not provided, the default value is assumed. If some sub-blocks are not included, that portion of design is not performed by SFDP.

B. How To Run SFDP

When the program is called, it asks for input file name. Then it asks for output file name. Then the user is given a message to wait till the processing is complete. When the design is over, a message is generated. While processing, if some errors occur, a message is generated and the program is terminated.